SOFT-SWITCHING SOLID-STATE TRANSFORMER FOR TRACTION APPLICATIONS

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SOFT-SWITCHING SOLID-STATE TRANSFORMER FOR TRACTION APPLICATIONS

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Dedicated to
my beloved parents and wife.

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TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

SUMMARY

Conventionally, power converters in traction systems interface with the medium-voltage (MV) catenary through a low-frequency transformer (LFT) operating at 16.7 Hz/50 Hz/ 60 Hz. The LFT converts the MV AC to low-voltage (LV) AC where low-voltage-rated power electronics are used to convert the LV AC to DC to interface with traction motor drives. However, the LFTs are heavy and less efficient. The drawbacks of the conventional traction converters can be overcome by the next-generation traction converters. In the next-generation traction converters, instead of using an LFT to interface with MV AC grid, MFT-based converters are used.

Due to their attractive features, the MFT-based traction converters have attracted significant research interest and multiple topologies have been investigated. With the advent of SiC devices, the performance of those converters can be further improved. However, simple drop-in replacement of Si devices with SiC ones can result in issues such as electromagnetic interference (EMI) caused by large dv/dt (30-50 kV/μs). A novel soft-switching-solid-state transformer (S4T) has been proposed in previous work to offer significant benefits including absence of switching losses, reduced and controlled dv/dt , and benign fault modes for MV applications. Because of the superior advantages of the S4T over the traditional voltage-source converters (VSCs), modular-S4T (M-S4T) is a promising candidate for the next-generation traction converters. Reverse-blocking (RB) devices are used as the main switching and resonant devices in the S4T. However, very little is known about the detailed behavior of such RB devices, especially when used in current-source converters (CSCs) with zero-voltage switching (ZVS).

To control the M-S4T and maintaining the voltage sharing between series-connected S4T modules, a novel fast dynamic control algorithm called model predictive priority-based switching (MPPS) has been proposed in previous work. Although the fast dynamic control algorithm is developed, due to deadbeat control feature of the MPPS control, any

delay in the communication between the S4T modules will have an adverse impact on the converter performance. Therefore, a control architecture using the MPPS is required to operate the M-S4T to achieve stable operation and fast transient performance.

In addition, despite significant work in HIL simulation of VSCs, there is very little knowledge about HIL simulation for CSCs with small energy storage element using fast dynamic control.

Considering the lack of knowledge of the M-S4T in the aforementioned areas, this dissertation presents deep investigation of the M-S4T for traction applications with clear understanding, solution and improvement to the aforementioned shortcomings including investigation of the power devices and design/ verification of control architecture as well as optimization of the converter.

CHAPTER 1
INTRODUCTION

1.1 Introduction to Traction Systems

Railway vehicles are powered by single-phase AC grids of 15 kV/16.7Hz or 25 kV/50Hz/60Hz or DC grids of 750V or 1500V [1–3]. The input voltages of the railway grids are summarized in Table 1.1. Depending on the classification of the vehicles and geographical location, different types of grids are utilized. Fig. 1.1 shows a general classification of railway vehicles and their corresponding grids [4, 5]. Light-rail vehicles (LRVs) are used in urban applications and are generally powered by a DC grid [6]. Locomotives are powered by a central traction system interfacing with a single-phase AC grid [7]. However, electric multiple units (EMUs), in contrast to locomotives, use a distributed traction system comprised of multiple motored vehicles [2, 8]. The comparison between locomotives and EMUs is shown in Fig. 1.2. Conventionally, when interfacing with a single-phase AC grid, a low-frequency transformer (LFT) is used. However, the LFT is heavy and bulky [9]. In [10], it is reported that the LFT occupies 15% of the total weight of the vehicle, showing that the converters using LFTs cannot meet the requirements for the next-generation traction converters [9, 11–13]. Therefore, the alternative converters using medium- or high-frequency transformers (MFT/HFT), which significantly reduce the size and weight, are promising

Table 1.1: Input voltage of the railway grid

Type of a system	Lowest voltage	Nominal voltage	Highest voltage
DC, 600V	400 V	600 V	720 V
DC, 750V	500 V	750 V	900 V
DC, 1.5 kV	1 kV	1.5 kV	1.8 kV
DC, 3 kV	2 kV	3 kV	3.6 kV
AC, 15 kV 16.7 Hz	12 kV	15 kV	17.25 kV
AC, 25 kV, 50 Hz	19 kV	25 kV	27.5 kV

for next-generation traction converters.

1.2 Solid-state Transformer for Traction Systems

Conventionally, converters in traction applications interface with medium-voltage (MV) catenary through a low-frequency transformer (LFT) operating at 16.7 Hz/50 Hz/ 60 Hz. The LFT converts the MV AC to low-voltage (LV) AC where low-voltage-rated power electronics are used to convert the LV AC to DC to interface with traction motor drives. However, the LFTs are heavy and less efficient [14]. In the next-generation traction con-

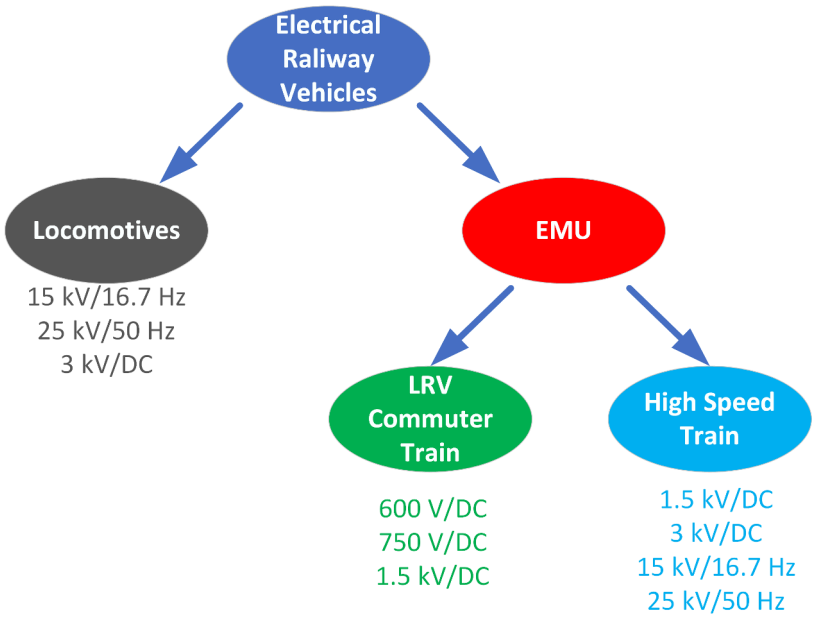


Figure 1.1: Classification of railway vehicles.

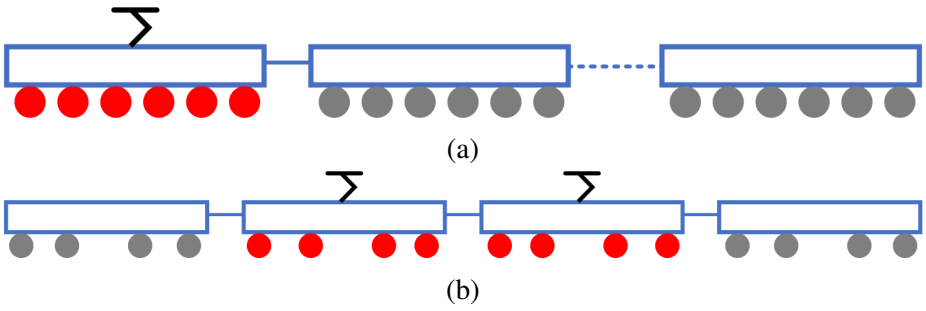


Figure 1.2: Comparison between (a) locomotives and (b) EMUs.

verters, instead of using an LFT to interface with MV AC grid, MV power electronics converters are used. The concept of using MFT-based traction converters, which is also known as solid-state transformer (SST), has attracted increased attention for traction systems as compared to the onboard line-frequency transformers [1]. Within the SST, series-connected power electronics devices or converters are used to interface the MV grid [13, 15–18]. This forms the active front-end (AFE) of the next-generation traction converters. The isolation between the MV side to the LV side is provided by the MFT in the second stage after the AFE. Due to the increase in the operating frequency, the size and volume of the MFT as well as other passive components can be reduced [14, 19]. MFT-based traction converters offer other several advantages including bi-directional power flow, multi-port operation, power quality control, compact size, and high efficiency [1].

1.3 Soft-switching Solid-state Transformer

1.3.1 Basics of Operation

A recently proposed current-source-based zero-voltage switching (CS-ZVS) converter with modularity and scalability features, i.e., soft-switching-solid-state transformer (S4T) has been shown to offer significant benefits including absence of switching losses, reduced and controlled dv/dt , and benign fault modes [20, 21], for MV applications. Fig.1.3 shows the topology of the S4T for three-phase applications.

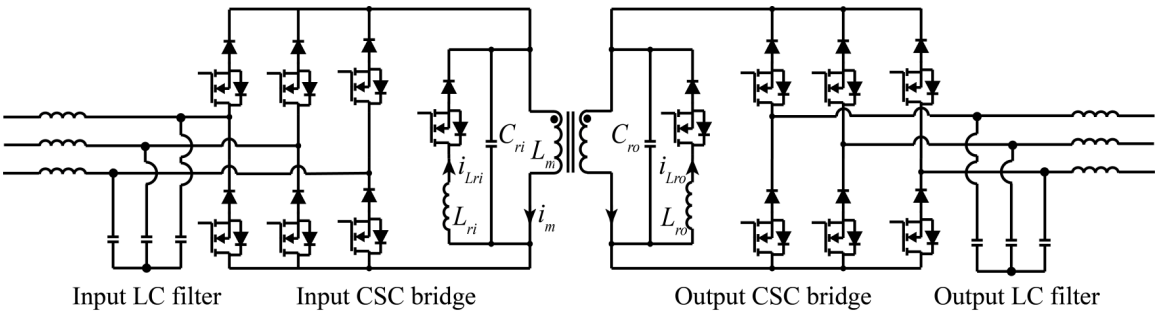


Figure 1.3: Circuit diagram of the three-phase soft-switching solid-state transformer (S4T) [20].

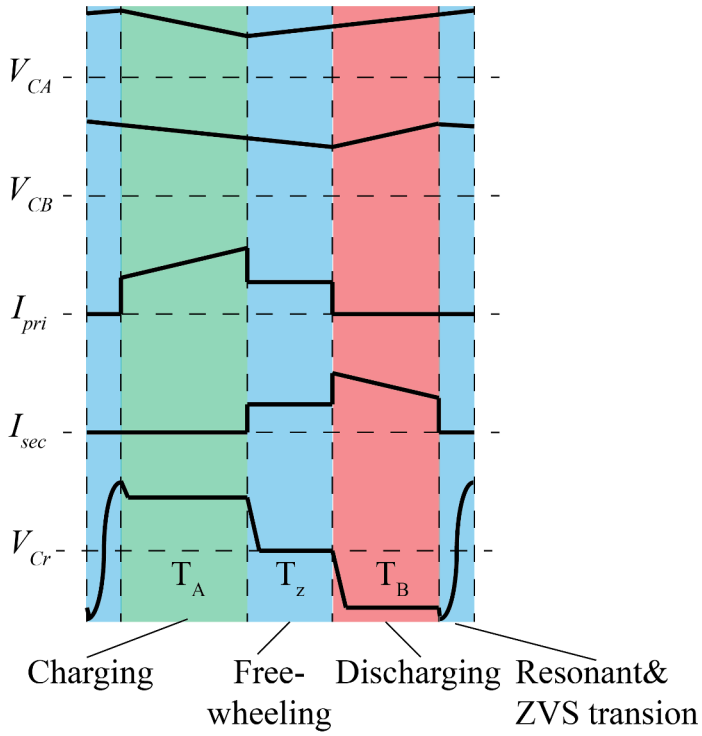


Figure 1.4: Operating principle of the S4T [20].

The S4T is a universal converter, which can be configured to convert a single- or 3-phase AC or DC input to a single- or a 3-phase AC or DC output, with bidirectional power transfer and buck-boost capabilities. The S4T is a minimal topology consisting of a single-stage solid-state transformer with a current source converter (CSC) on both sides of an MFT/HFT featuring relatively low magnetizing inductance (L_m), and an auxiliary resonant circuit to achieve ZVS [20]. As shown in Fig. 1.4, the basic operation of the S4T converter has two cycles- a forward cycle, where energy is transferred from the sending terminal and is stored in L_m, and a regen cycle where energy is transferred from L_m to the receiving terminal. The two active states are interposed with state transition and/or resonant state, which aid in achieving ZVS of all the semiconductor devices [20]. The ZVS process of the S4T can be further explained in Fig. 1.5.

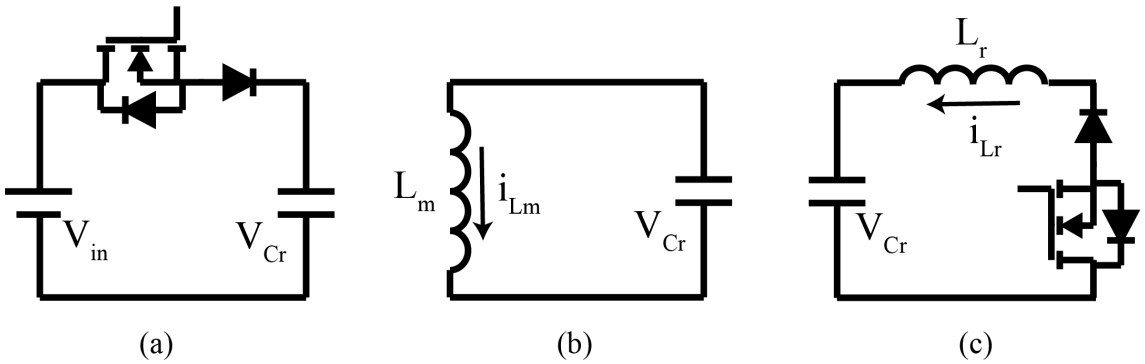


Figure 1.5: Equivalent circuits of the S4T during (a) ZVS turn on, (b) ZVS transition, and (c) resonant capacitor reset.

1.3.2 Control of M-S4T

Passive components, such as electrolytic DC-link capacitors or inductors, occupy more than 20% of the size and weight of a power converter [22, 23]. Improving reliability and reducing size and weight of the converters are becoming essential design requirements for next-generation power converters. To this end, decreasing the DC-link energy storage and employing smaller components can contribute to meeting those requirements [24–26]. Such a converter with a small DC-link energy storage is referred to as a low-inertia converter [24]. The major hindrance in reducing the stored energy in the passive components is the increased coupling and interactions between the input and output stages, which consequently leads to a more complex and challenging control, when compared to the conventional converters. When the low-inertia converters are operating in a stacked mode like in MV power converters [27], the dynamic voltage sharing amongst the series-connected modules becomes challenging and the voltage balancing problem must be addressed using fast dynamic control. Such a multi-objective, multi-degree of freedom control problem and the challenges associated with realizing the control requirements by using classical controllers such as proportional-integral-based (PI) controllers to achieve fast dynamic performance and stable operation of the stacked low-inertia converters is discussed in [28]. To control the M-S4T and guarantee voltage sharing among series-connected S4T modules, a novel fast dynamic control algorithm called model predictive priority-based switching

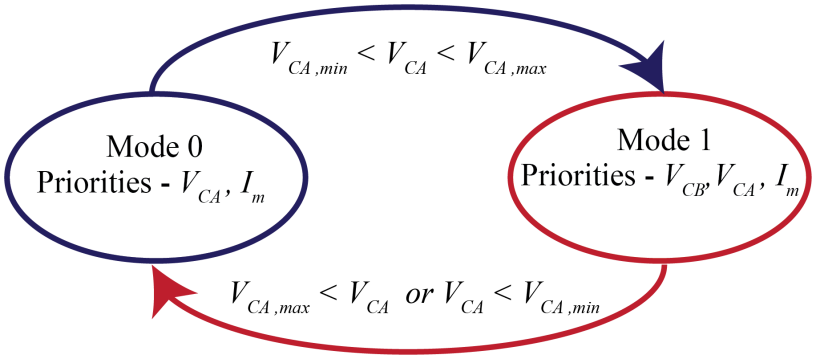


Figure 1.6: MPPS control algorithm[28].

(MPPS) has been proposed in the previous work [28], as shown in Fig. 1.6.

1.3.3 Hardware-in-the-loop Simulation

Hardware-in-the-loop (HIL) simulation of power electronics systems is a way to enable part or all of the power electronics converters simulated with signal-level data transferred or saved. Real-time (RT) modelling and simulation with controller hardware-in-the-loop (CHIL) helps to investigate and verify fast control algorithms. The simulation platforms like Opal-RT help to increase the simulation speed compared to MATLAB/Simulink sim-

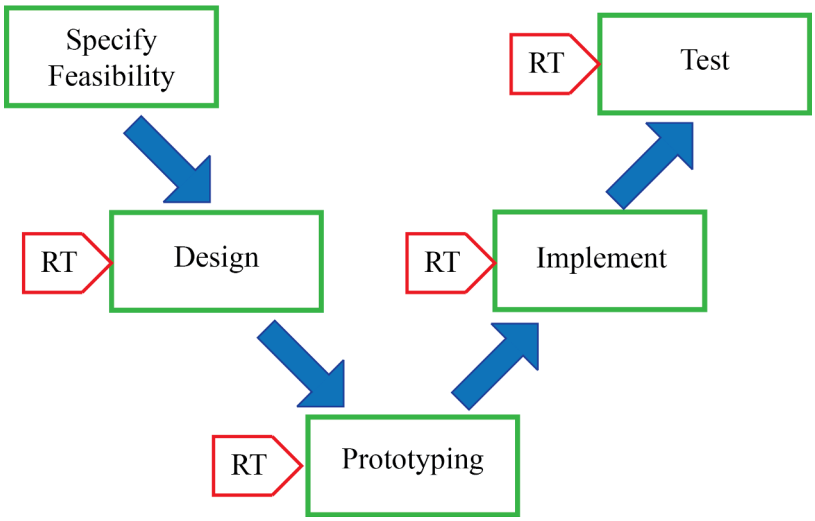


Figure 1.7: Application of RT HIL simulation in multiple stages of power converter development [29].

ulation in a single-core desktop computer [30–32]. HIL simulation is shown to accelerate the prototyping process, debug the control algorithms as well as test corner cases of the converter, as shown in Fig. 1.7. Due to the attractive features of HIL simulation, significant work of HIL simulation based on VSCs has been implemented. However, in most of the HIL implementation of VSCs, conventional PI controller is used. Because of the fast-dynamic nature in low-inertia converters, all the non-linearities and delays become significant in implementing such control algorithm. Therefore, HIL implementation of conventional PI-controlled VSCs is not applicable to low-inertia converters using fast dynamic control.

1.4 Problem Statement

Due to the attractive features of SSTs for traction application, significant research work has been done in this area. With the advent of SiC devices, the performance of the converters in SSTs can be further improved. However, simple drop-in replacement of Si devices with SiC ones can result in issues such as electromagnetic interference (EMI) caused by large dv/dt (30-50 kV/μs). Because of the the superior advantages of the S4T over the traditional VSCs, the M-S4T is a promising candidate in the next-generation traction converter. Reverse-blocking (RB) devices are used as the main and resonant devices in the S4T. Previous work related to the S4T/ M- S4T has already verified its basic operation along with the control algorithm of the M-S4T. However, very little is known about the detailed behavior of such RB modules, especially when used in CSCs with ZVS.

Although a fast dynamic control algorithm is developed, due to deadbeat control feature of the MPPS control, any delay in the communication among the S4T modules will have an adverse impact on the converter performance. Therefore, a control architecture using the MPPS is required to operate the M-S4T to achieve stable operation and fast transient performance.

To verify the fast dynamic control algorithm and control architecture, a simulation plat-

form is required. HIL can accelerate the simulation and evaluate the impacts of the non-idealities of the controller. Although significant work has been done for HIL simulation of VSCs, there is very little knowledge about HIL simulation for CSCs with small energy storage element using fast dynamic control.

1.5 Objective of the Research

This dissertation presents deep investigation of the M-S4T for traction applications with clear understanding, solution and improvement to the aforementioned shortcomings. The proposed research will focus on the following aspects:

- RB-device performance under both hard-switching and soft-switching conditions;
- Practical concerns for use of RB-device in S4T converter;
- HIL modeling of S4T for real-time simulation;
- Control architecture enabling fast communication between modules;
- Design of the S4T and trade-off among system variables.

1.6 Chapter Outline

This dissertation is organized as the following:

- Chapter 2 will present a comprehensive literature review of the state-of-art traction converters, including previous work on MV device characterization, HIL of power converters, etc.
- Chapter 3 will introduce multiple different configurations of the M-S4T to achieve the next-generation traction converters. The configurations will be discussed and compared and the most promising one will be selected.

- Chapter 4 will first presents the loss characterization of the SiC RB module under both hard-switching and soft-switching conditions. Then, the phenomenon during switching transients will be analyzed and discussed. The loss mechanism of the SiC RB module under soft-switching condition will be presented.

- Chapter 5 will present practical considerations of RB module in the S4T. All of the devices in the S4T including main and resonant devices will be discussed. A gating strategy that can fully exploit the benefit of the S4T will be presented.

- Chapter 6 will present the implementation challenges of HIL simulation of the S4T and M-S4T. A novel modeling method of the M-S4T is proposed to use the existing HIL platform for simulation.

- Chapter 7 will present design considerations of the control architecture of the M-S4T. A new control architecture for low-inertia stacked converters is proposed.

- Chapter 8 will present the design tradeoffs among multiple system-level parameters including power level per each module, switching frequency, etc.

- Chapter 9 will present the application of the proposed methodologies to a full-scale traction converter.

- Chapter 10 will summarize the dissertation and present the potential future work based on this research.

CHAPTER 2

LITERATURE REVIEW AND PREVIOUS WORK

2.1 Conventional Traction Converters

Conventionally, the power electronics converters in traction applications interface with the MV catenary through an LFT operating at 16.7 Hz/50 Hz/ 60 Hz. The LFT converts the MV AC to LV AC where low-voltage-rated power electronics are used to convert the LV AC to DC to interface with traction motor drives. Connection of the conventional LFT-based traction converter is shown in Fig. 2.1. However, the LFTs are heavy and less efficient [1–3].

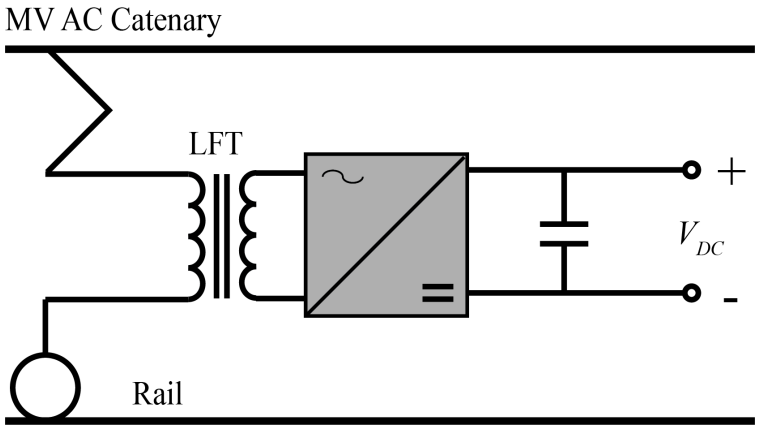


Figure 2.1: Interfacing the conventional traction converters using a low-frequency transformer (LFT) [33].

2.2 Next-generation Traction Converters

The drawbacks of the conventional traction converters can be overcome by the next-generation traction converters, where instead of using an LFT to interface with the MVAC grid, MFT-based converters are used, as shown in Fig. 2.2. The comparisons of the key features of the LFT-based conventional traction converters and the MFT-based next-generation

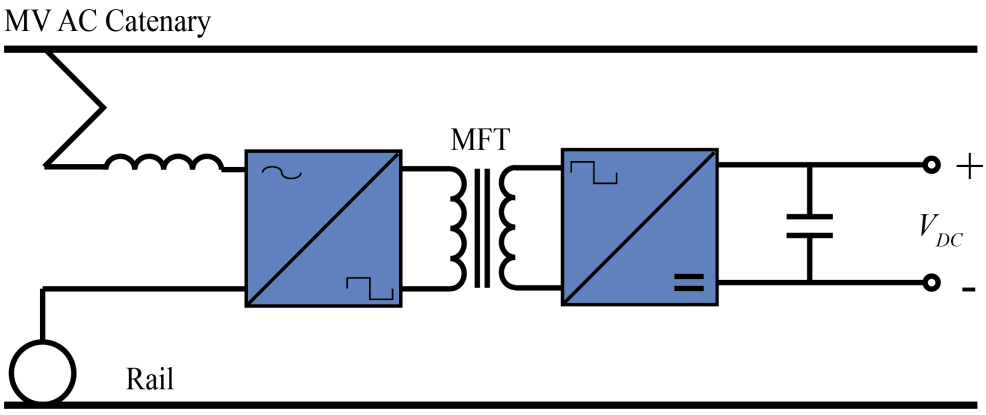


Figure 2.2: Next-generation traction converters using a medium-frequency transformer (MFT) [33].

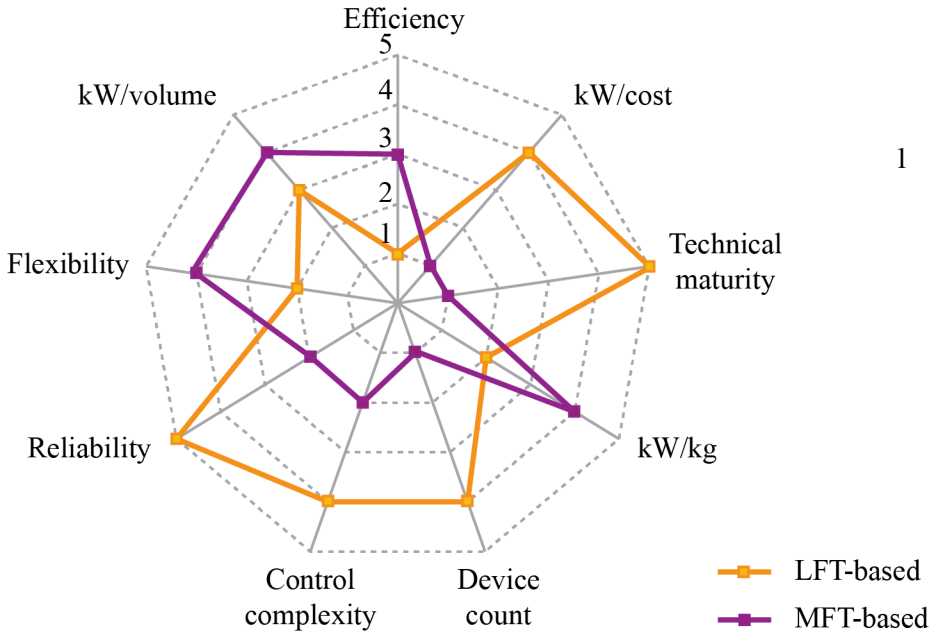


Figure 2.3: Comparison between the LFT-based and MFT-based traction converters [2].

traction converters are shown in Fig. 2.3. It is shown that the LFT-based converters have less device count and cost, matured technologies and higher reliability compared to the MFT-based converters. However, it cannot meet the requirements of the next-generation traction converters [9, 11–13]. The MFT-based converters, also known as SSTs, can significantly improve the performance of the converters in terms of power density, efficiency, and flexibility. Due to the attractive features provided by next-generation traction converters in

traction applications, the MFT-based traction converters have attracted significant research interest. In the technical literature, significant work on the MFT-based traction converters has been done. The state-of-the-art MFT-based traction converters can be further classified into four categories:

- Two-stage single-phase AC-DC-DC conversion topologies [10, 34–42];
- Cyclo-converter-based single-stage single-phase AC to DC conversion [43].
- Modular multilevel converter (MMC)-based single-stage single-phase to 3-phase AC conversion [44–46];
- CSC-based single-stage single-phase AC to DC conversion [47, 48].

2.2.1 Two-stage Single-phase AC-DC-DC Conversion

These topologies are all based on a two-stage configuration in which an AC-DC converter is followed by a DC-DC converter with galvanic isolation. To interface with the MV AC grid, the traction converters are connected in an input-series-output-parallel (ISOP) configuration, as shown in Fig. 2.4. On the input side, the converters are connected in series to meet the input voltage requirement, which is also known as AFE. On the output side, the converters are connected in parallel to meet the power requirement.

In [34], the authors utilize a cascaded H-bridge (CHB) as the AFE to interface with the single-phase MV AC grid. The AFE is followed by a series-resonant converter (SRC) isolated by MFT/HFT. The SRC ensures ZVS of all the devices in the SRC converter when operating at MF or HF. Reference [35] utilizes a similar circuit with the SRC replaced by an LLC converter. The voltage balancing of the AFE is achieved passively using a bulky capacitance and open-loop control of the LLC converter. This converter has been verified on the actual locomotive in Switzerland. With a similar topology, the LLC converter is changed to a dual active bridge (DAB) converter in [36]. In contrast to the passive voltage balancing in [35], reference [36] uses an active voltage balancing. The voltage is balanced

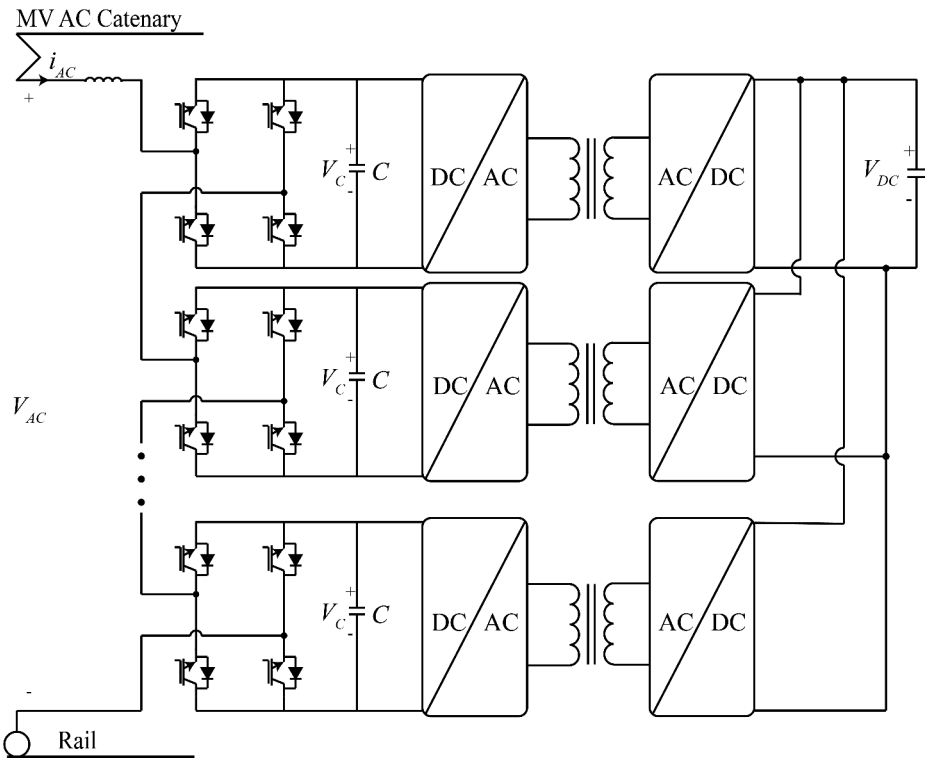


Figure 2.4: Input-series output-parallel configuration for traction converters interfacing MV grids.

by actively changing the transferred power of each module. In all these converters, the DC-DC stage operates under soft-switching condition within a limited load range while the devices in the AFE are hard switched. This leads to additional switching losses and EMI issues, although the switching frequency is relatively low in this stage.

2.2.2 Cyclo-converter-based Single-stage Single-phase AC to DC Conversion

A cyclo-converter-based traction converter is proposed in [43], as shown in Fig. 2.5. On the primary side of the transformer, the cyclo-converter converts the single-phase low-frequency AC to medium-frequency AC. On the secondary side of the transformer, a full-bridge converter is used to convert the medium-frequency AC to DC. However, in this converter, the transformer is operated at 400 Hz, which is smaller than the operating frequency of the other topologies.

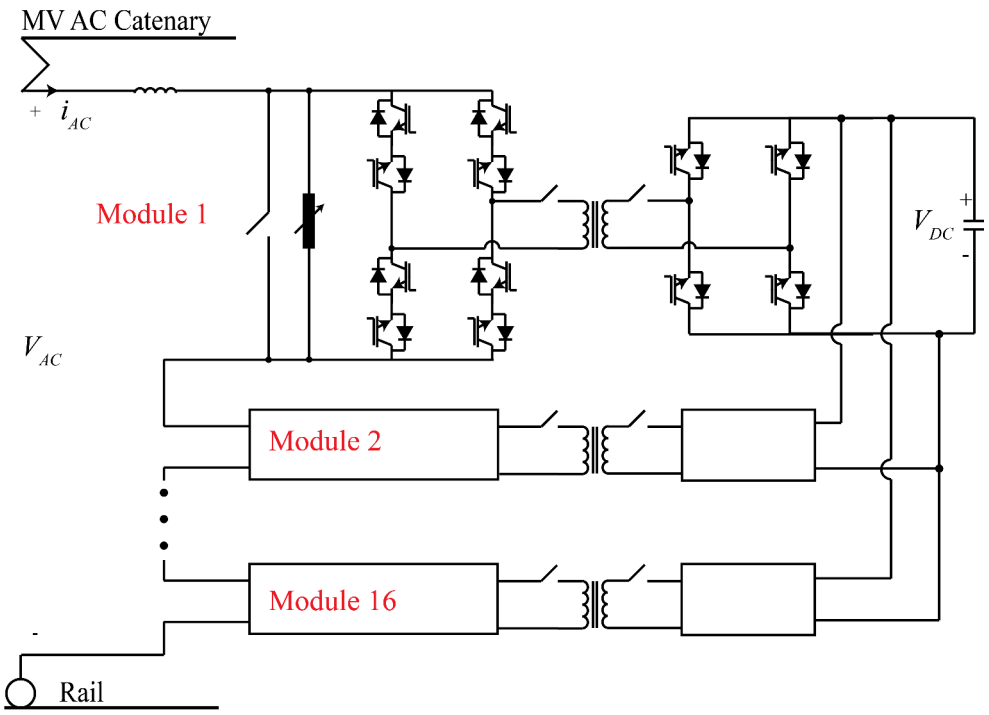


Figure 2.5: Cyclo-converter-based traction converter [1, 43].

2.2.3 MMC-based Single-stage Single-phase AC to DC Conversion

Another family of the next-generation traction converters is based on MMC topology, as shown in Fig. 2.6. On the primary side of the MFT, the MMC converts the low-frequency AC to medium-frequency AC while on the secondary side of the MFT, a full bridge is used to convert the medium-frequency AC to DC. Unlike the previously mentioned topologies, in [44–46], only simulation results are reported without any experimental verification. This topology merges the advantages of MMC topology [49, 50], however, the switching devices operate under hard-switching condition.

2.2.4 CSC-based Single-stage Single-phase AC to DC conversion

Another CSC-based traction converter is shown in Fig. 2.7 in which the MFT/HFT magnetizing inductor is acting as the energy transferring element of the converter and the operation is similar to a fly-back converter. However, unlike the previous VSCs in ISOP

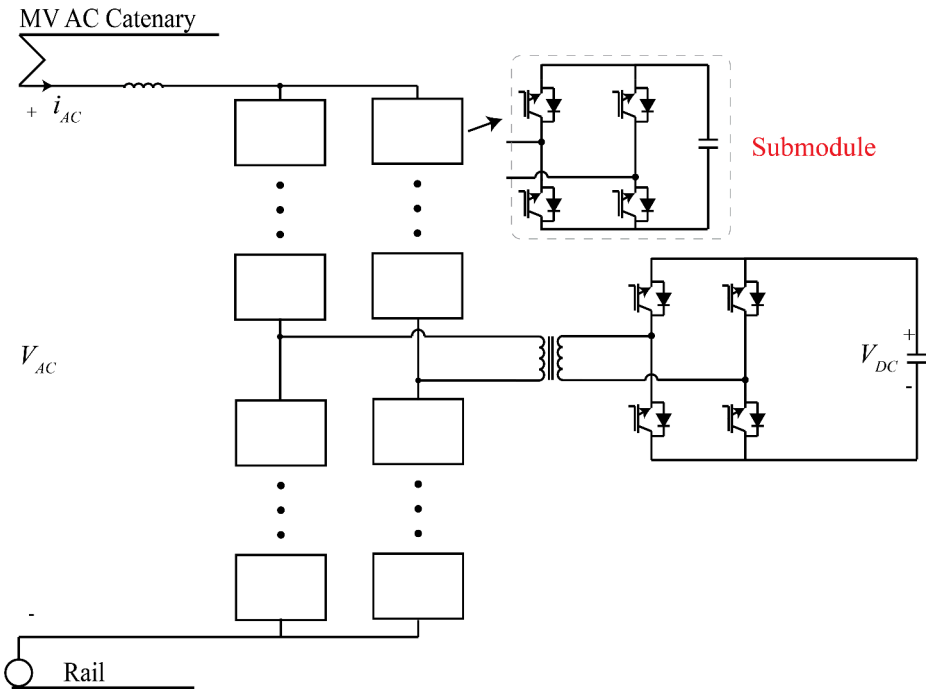


Figure 2.6: MMC-based traction converter [1, 44].

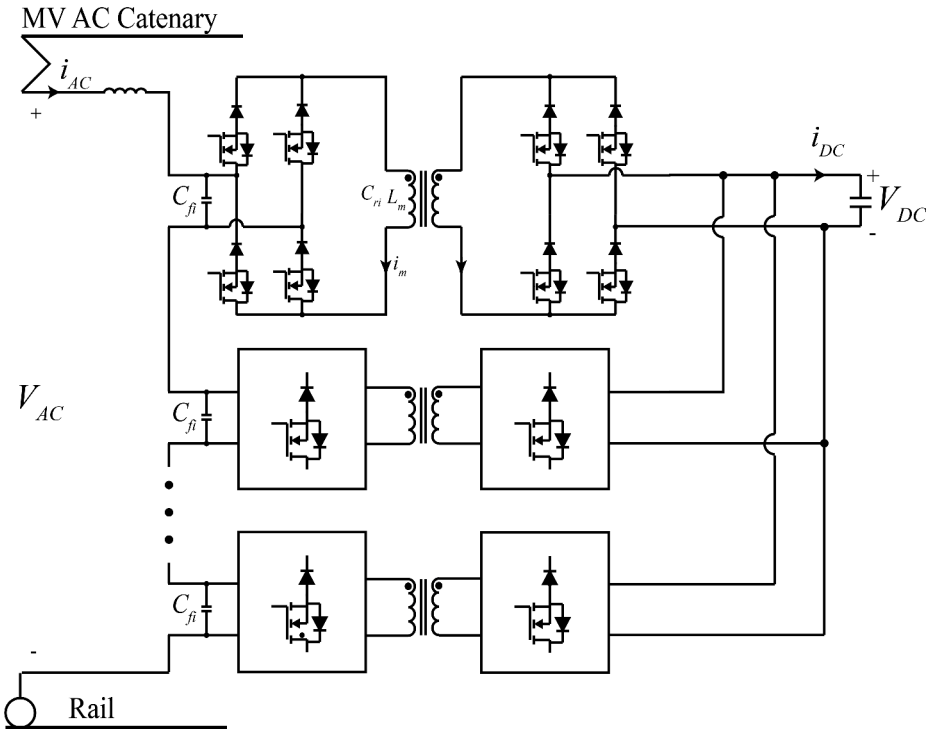


Figure 2.7: Current-source converter-based traction converter [47].

configuration, this converter operates under hard-switching condition. Therefore, the efficiency and EMI performance of this converter is compromised. The features of all the traction converters are summarized in Table. 2.1.

2.2.5 Admittance of Traction Converters

For traction applications, harmonic instability can occur when a large number of railway vehicles are operating in the railway grid [51]. Excessive harmonic currents are injected into the grid when a large number of railway vehicles feed energy to the grid at similar frequency. The poorly damped harmonic resonances in the grid can lead to equipment damage and even collapse of the grid. Therefore, enough damping should be provided by the traction converter, which poses requirements on the input admittance of traction converters. The measurement of admittance is shown in Fig. 2.8. In order to maintain a stable grid operation, the real part of the input admittance is required to be positive [35]. In [35], a feed-forward loop is added to the control algorithm, which can maintain the admittance of the traction converter positive for all frequencies.

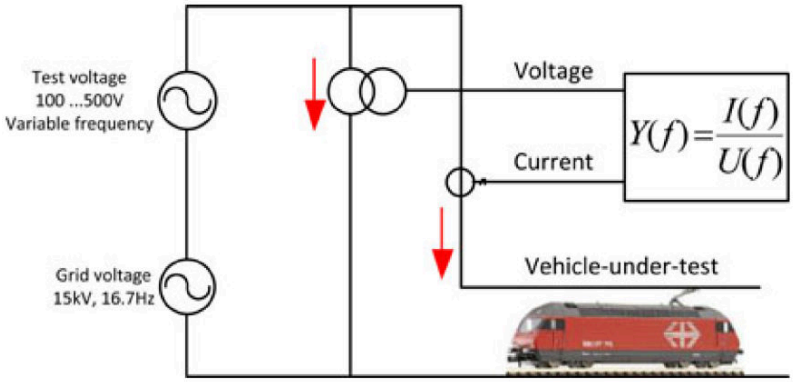


Figure 2.8: Admittance measurement method [35].

Table 2.1: Summary of traction converter topologies

References	[35, 38]	[42]	[34]	[41]	[43]	[46]
First stage topology	CHB (MVAC-DC)				Cycloconverter (MVAC-MFAC)	MMC (MVAC-HFAC)
Second stage topology	LLC	SRC			FB	FB
Year	2012	2002	2007	2007	2007	2004
Input voltage	15 kV/16.7 Hz	15 kV/16.7 Hz	15 kV/16.7 Hz	15 kV/16.7 Hz	15 kV/ 16.7 Hz	15 kV/16.7 Hz
Power	1.2 MVA	350 kVA	1.5 MVA	3 MVA	1.2 MVA	2 MVA
Efficiency	96%	99.3%				
Switching frequency	CHB: 500Hz/ LLC: 1.75 kHz	SRC: 10 kHz		CHB: 550 Hz/ SRC: 8kHz	400 Hz	4 kHz
Soft-switching	Yes	Yes	Yes	Yes	Yes	No
MV side device	6.5 kV IGBT		6.5 kV IGBT	6.5 kV IGBT	3.3 kV IGBT	3.3 kV IGBT
Number of modules	8	12	8	8	16	8 / arm

2.3 MV/HV Semiconductor Devices

2.3.1 Series-connection of LV Devices

Realization of MV converters based on low-voltage Si devices necessitates series-connection of semiconductor devices, which in turn increases the complexity in control and deteriorates the efficiency [52, 53]. In [54, 55], an active gate control method is developed to maintain voltage sharing between series-connected IGBTs. In [56], an auxiliary circuit is designed to assist both steady-state and dynamic voltage sharing across series-connected devices passively. In addition, a snubber circuit is designed in [57] to maintain the voltage sharing. Fig. 2.9 summarizes different methods for voltage sharing in series-connected devices.

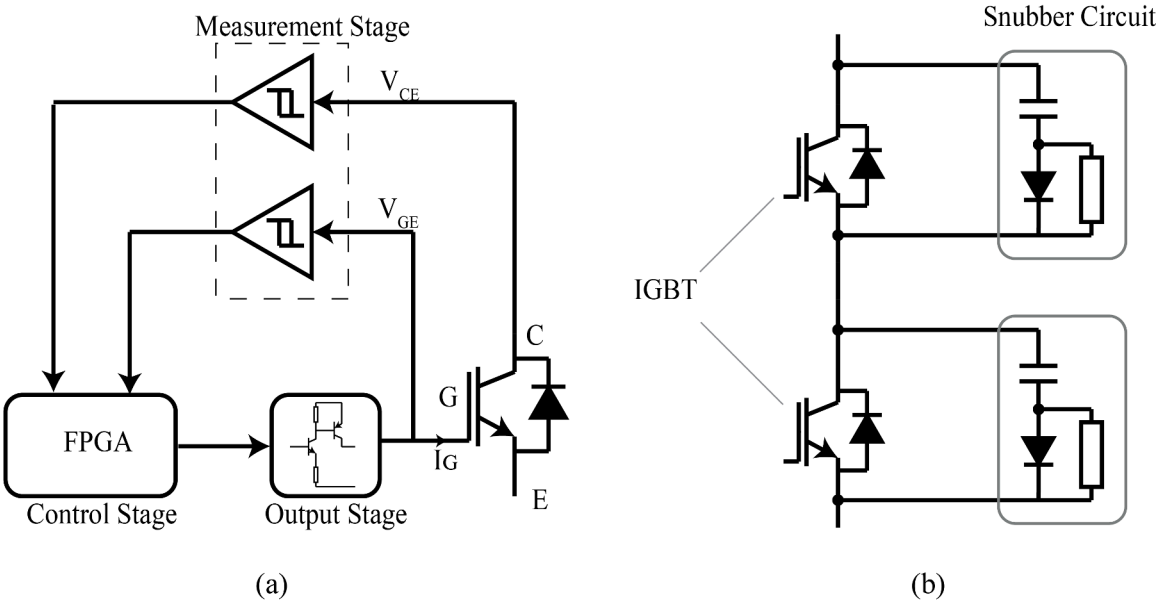


Figure 2.9: Existing methods for voltage sharing in series-connected devices (a) active gate control [54] and (b) auxiliary snubber [56].

2.3.2 Comparison between SiC and Si Devices

Although the aforementioned existing methods can solve the voltage sharing issue when using low-voltage devices in high-voltage applications, control and circuit complexity, and

cost as well as power losses increase. Alternatively, the use of a single medium-/high-voltage device is preferred in the MV/HV applications. In [58], the use of 3.3 kV and 4.5 kV Si IGBTs for the MV application are discussed and it is shown that the switching frequency range of the MV/HV Si devices is limited to below 1 kHz. Operating the Si IGBT under 1 kHz dramatically impacts the size and performance of the converter [59]. Silicon Carbide (SiC) devices, compared to their Si counterparts, offer superior electrical and thermal characteristics in terms of efficiency, power density, switching frequency, and operating temperature [60–65]. Comparison of wide bandgap devices including SiC and GaN devices with Si devices in terms of electrical and thermal performance is summarized in Fig. 2.10. The summary of comparison of switching characteristics of MV/HV SiC and Si devices is listed in Table. 2.2.

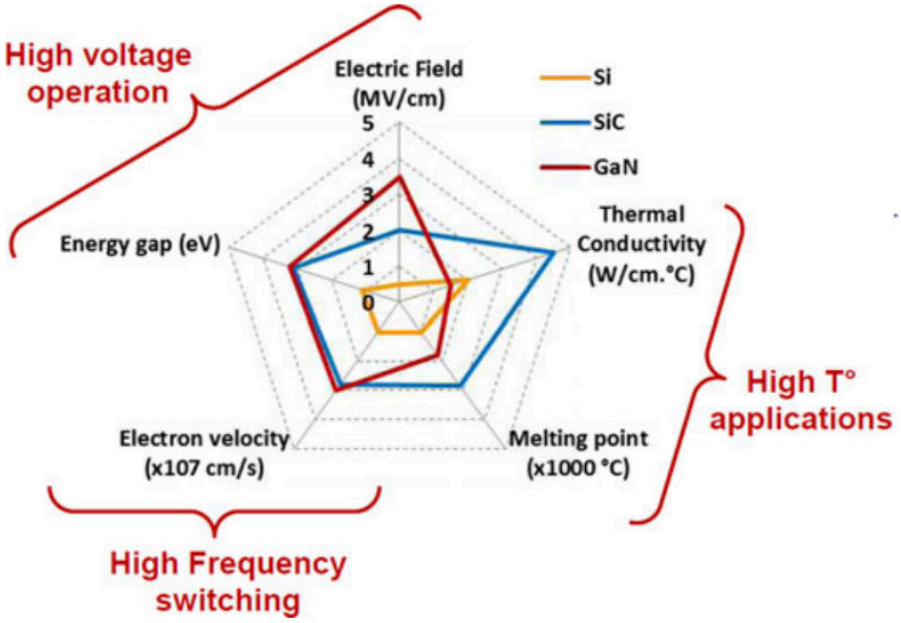


Figure 2.10: Physical characteristics of Si and wide bandgap devices [60].

SiC devices rated at $>$ 3.3 kV and 50-200 A can simplify the design of MV and HV converters [66–71]. Reference [66] shows the performance of a 3.3 kV 400 A SiC MOSFET. The advantages of using this power module over the conventional Si devices as well as SiC devices with lower voltage ratings is shown in Fig. 2.11. In [68], a 10 kV SiC MOSFET is

Table 2.2: Comparison of switching data of MV Si and SiC devices [64].

Device	Vce(on)	Switching time		Eloss	
	Vce(on)	Ton (ns)	Toff (ns)	Eon (mJ)	Eoff (mJ)
6.5 kV 10 A Si-IGBT and Dioe	2.5	590	5250	8.24	52.9
6.5 kV 10 A Si IGBT and SiC-JBS Diode	2.75	490	5100	3.34	48.5
10 kV 10 A SiC-MOSFET and SiC-JBS Diode	5.95	590	200	3.7	0.23

characterized and experimentally demonstrated in a converter prototype. However, simple drop-in replacement of Si devices with SiC ones can result in issues such as EMI caused by large dv/dt (30-50 kV/μs) [72]. Fig. 2.12 shows significant ringing caused by the loop inductance and device parasitic capacitance under hard-switching condition. Besides ringings, it is shown that a gate-source resonance exists because of the common-source inductance. This resonance could exceed the gate voltage rating if the common-source inductance is too large. In addition, because of the fast switching speed of SiC devices, the high dv/dt can impact the operation of the complementary devices when the two devices are in phase-leg configuration, which is known as crosstalk [73]. In [74], an auxiliary circuit is proposed to solve the crosstalk issue for SiC as shown in Fig. 2.13. Although the circuit can assist in clamping the gate voltage during switching transitions, the circuit adds to complexity and additional losses and cost.

2.3.3 Reverse-blocking Devices

The RB device/module here refers to a standard switch and diode, connected in series either at die level or at discrete package level and not a fundamentally reverse blocking device [75], as shown in Fig. 2.14. However, very little is known about the detailed behavior of such RB modules, especially when used in CSCs with ZVS. References [76] and [77] discuss the behavior of RB SiC modules under hard-switching conditions. Reference

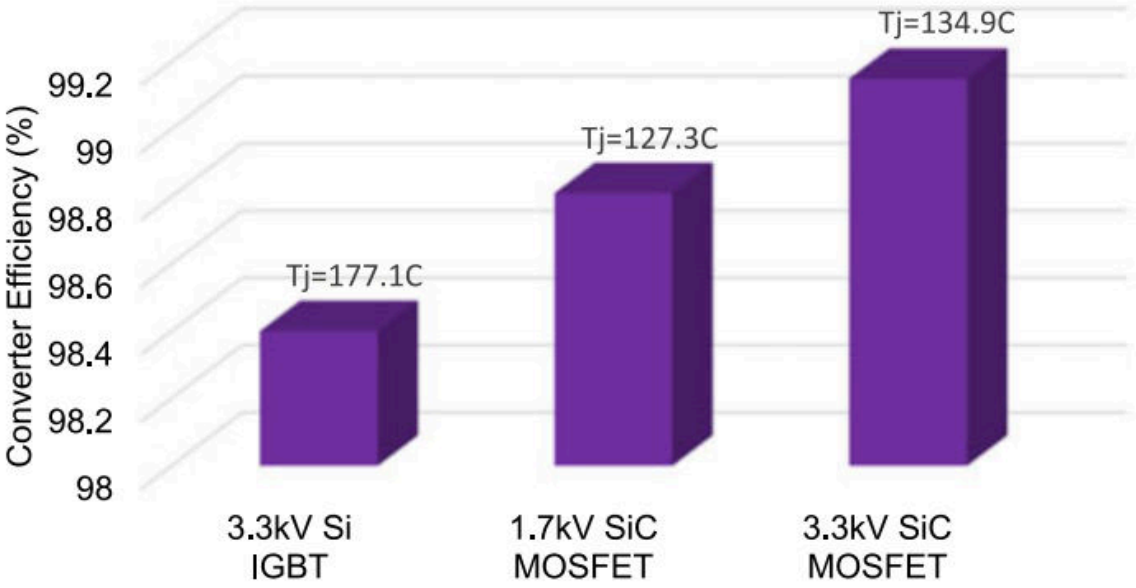


Figure 2.11: Total converter efficiency and maximum junction temperature of switches [66].

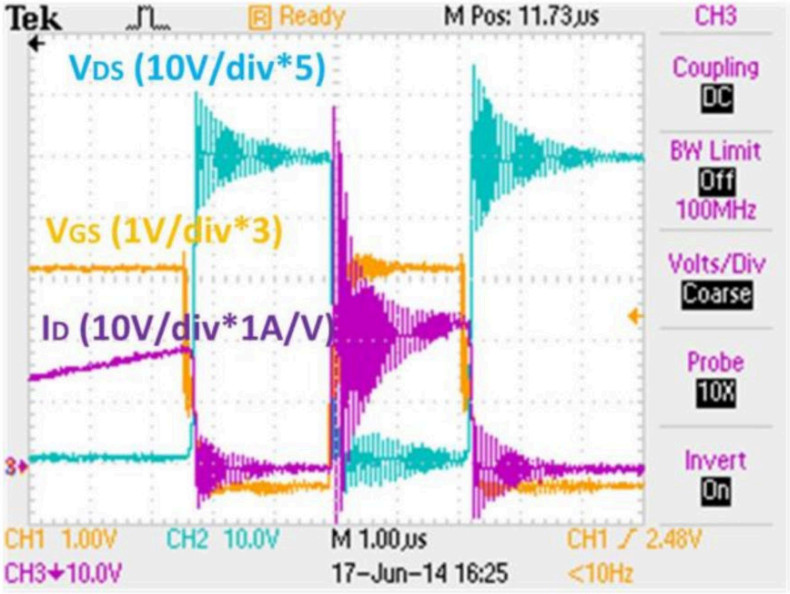


Figure 2.12: Voltage and current waveforms of a 1.2 kV SiC device under hard-switching condition [72].

[76] shows that some of the switching phenomena in RB devices are similar to those in the conventional Si devices in VSCs. It is shown that the power losses of the RB devices are

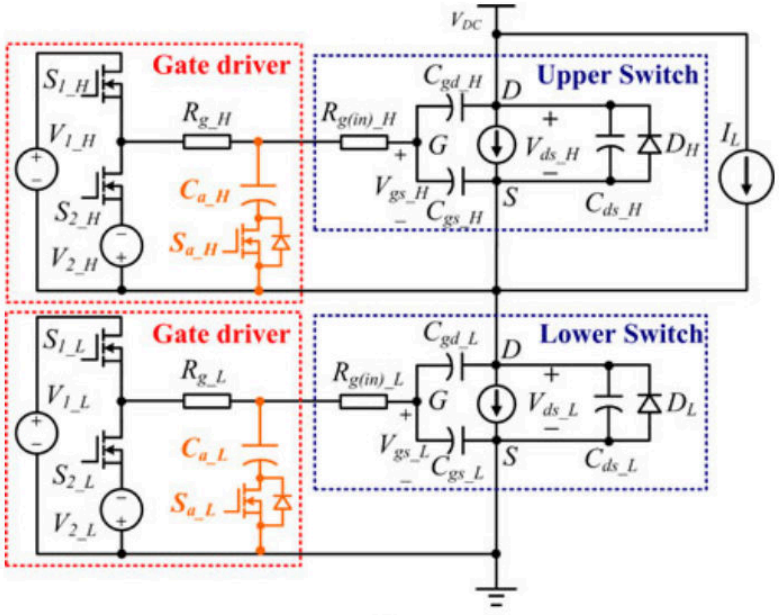


Figure 2.13: Active clamp circuit to suppress crosstalk phenomenon [74].

reduced when using SiC MOSFET and SiC diode in [77]. However, clear understanding of the characteristics and performance of RB SiC modules under soft-switching conditions have not been yet reported in the literature.

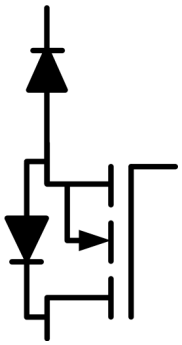


Figure 2.14: Configuration of a reverse-blocking module.

2.3.4 Cosmic Ray Impact on MV/HV Devices

Power electronics devices, especially MV/HV devices, are impacted by cosmic radiation [78–80]. It can impact the robustness and reliability of the power devices [79]. The

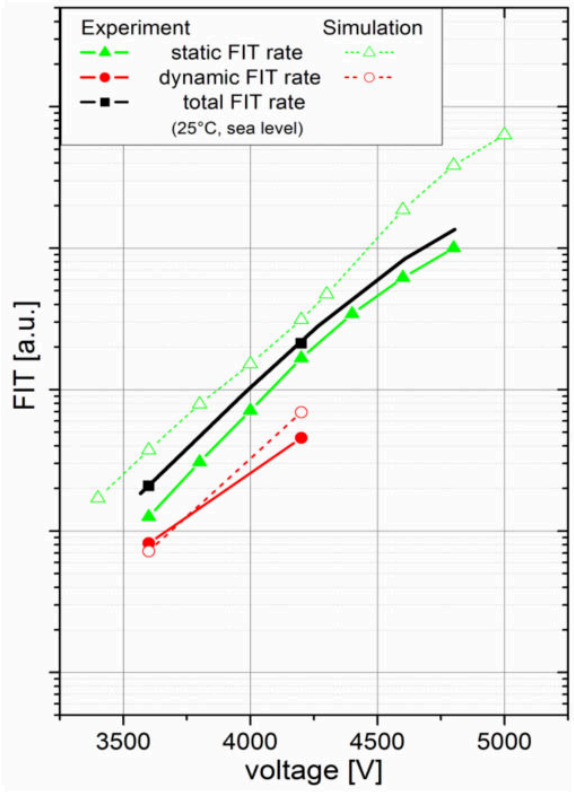


Figure 2.15: FIT for 6.5 kV devices under different blocking voltages [78].

failure mechanism is illustrated in [80]. Fig. 2.15 shows the failure in time (FIT) of 6.5 kV devices under the operating condition of different blocking voltages. It is shown that the FIT increases as the blocking voltage increases. Consequently, the recommended operating voltage for devices with different voltage ratings is summarized in Table. 2.3 and the number of modules is selected based on the operating voltage of the devices.

Table 2.3: Summary of the operating voltage of different devices

Device breakdown voltage	Operating voltage	Number of stages for 25 kV/ 50 Hz	Number of stages for 15 kV/16.7 Hz
3.3 kV	1.8 kV	23	14
4.5 kV	2.5 kV	17	10
6.5 kV	3.6 kV	12	7
10 kV	5.5 kV	8	5

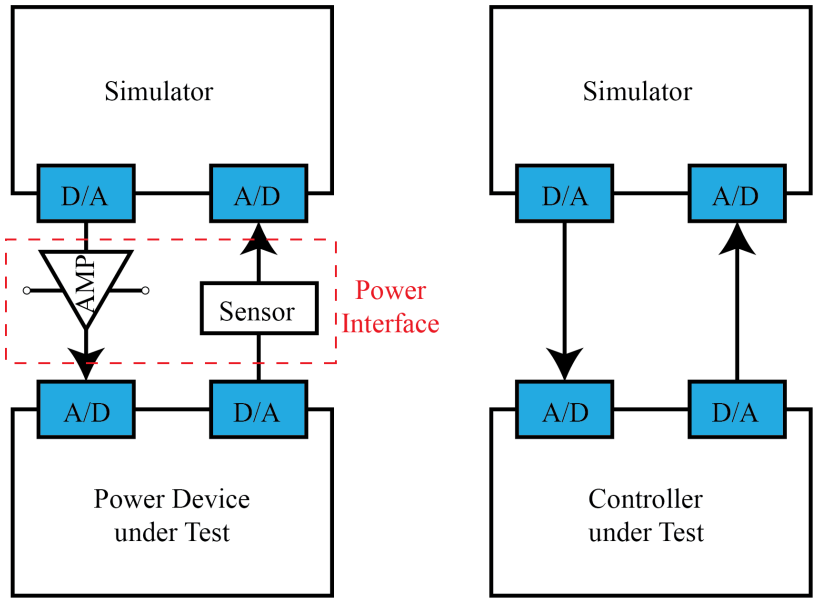


Figure 2.16: Comparison between (a) PHIL and (b) CHIL [81].

2.4 HIL Simulation for Power Converters

2.4.1 Overview of HIL Simulation

HIL simulation of power electronics is a way to enable part of the power electronics converters simulated while the other part is implemented. In [29], it is shown that HIL is capable of simulating transmission and distribution systems as well as multi-physics systems. Depending on the portion of system that is simulated, HIL can be further divided into power HIL (PHIL) and controller HIL (CHIL). In PHIL, some parts of a power converter are simulated while the rest are built and connected to the simulated parts through an amplifier. In CHIL, the whole power converter is simulated while its controller is built in hardware. The control signal can be connected to the simulated converter through I/Os. The difference between PHIL and CHIL is illustrated in Fig. 2.16. By using HIL, the converter is generally operating in real time, with the benefits including:

- Fast simulation speed: Because of its real-time nature, HIL simulation is in the order of 10 or 100 times faster compared to the traditional single-core simulators like

MATLAB/Simulink or PSCAD;

- Hardware interface: The performance of some hardware components can be evaluated by using HIL before their installation by the real hardware, i.e., the controllers in the converters can be fully checked under different operating conditions with considering the practical communication non-idealities between the micro-controller itself and the auxiliary circuits.

- Reduced risks with associated failure: Even though a failure may occur and damage the system, since only a part of the system is built based on high-cost power electronics, the damage is limited. In addition, the signal-level simulator is fully isolated from the power converter.

- Reduced cost: Although the HIL platform is expensive as an initial cost, it could reduce the cost of failures in the practical converters.

- Easy implementation and variation: Since part or all of the power electronics converters are simulated, assembly and installation work is much reduced in HIL when the configuration of the circuit or the parameters of some components are changed.

- Failure cases test: By changing the simulation conditions and circuit configuration, the converter system can also be simulated under any fault and failure cases. Compared to the additional protection circuits and power supplies needed in the real converter to simulate fault cases, HIL has no additional effort in this aspect.

2.4.2 State-of-the-art HIL Simulation for Power Converters

Due to significant advantages introduced by HIL simulation, it has been widely adopted in the design process of different power converters [81–89]. In [83], an induction machine drive model is implemented using HIL simulation. In [81], the interfacing issues with different simulators to the I/Os, and communication are addressed. In [82], the HIL

simulation is used in a hybrid wind turbine generator (WTG) and energy storage system (ESS), as shown in Fig. 2.17. The challenges introduced by the conventional VSCs and the switching event interpolation are well addressed in [82]. An example of WTG ESS simulation is successfully simulated on the OPAL-RT platform at a time step of 50 μs when the switching frequency is less than 2 kHz. In [85, 86], the control algorithm of an MMC is improved based on the HIL simulation where both of the converter and the controller are implemented in the OPAL-RT units. Most of the state-of-the-art HIL simulation are using PI based control algorithms, however, a model predictive control (MPC) is implemented in [85, 86]. Another HIL-based MMC design is shown in [87]. Unlike the HIL simulation in [85, 86], which is focused on the controller design, the approach in [87] focuses on the entire system design including the communication, control and protection. A modular multilevel DC-DC converter (M2DC) is implemented using CHIL simulation in [88] where a number of converter functionalities are verified using a customized controller. The connection between the customized controller and the simulator is achieved by using an interface card. In [84], an adaptive discretization method is proposed and verified on the two-level inverter. In [90], a PHIL simulation is implemented using an AC-DC converters.

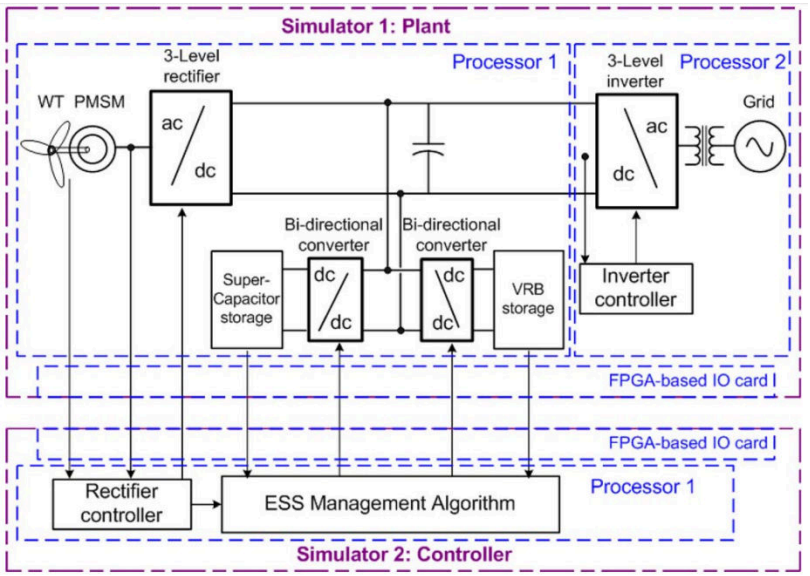


Figure 2.17: RT HIL simulation for a WTG ESS system [82].

A summary of the state-of-the-art HIL simulation is listed in Table. 2.4.

2.5 Conclusions

The literature review introduces the limitations of the conventional LFT-based traction converters and the need for the next-generation MFT-based traction converters. Different state-of-the-art topologies to achieve the next-generation traction converters are reviewed. All of the existing MFT-based traction converters cannot achieve soft switching for part or all of the power devices in the converter. In addition, most of the topologies are based on a multi-stage configuration, which leads to additional circuit complexity.

Considering the limitations in the existing MFT-based traction converters, the single-stage, fully soft-switched M-S4T is a promising topology for traction application. To achieve the M-S4T, MV SiC RB devices are used. However, understanding of the behaviour of the RB devices under soft-switching condition is limited. The loss mechanism and the practical concerns of using the RB devices need to be further investigated to fully utilize the benefits of the M-S4T.

To control the M-S4T, the MPPS can achieve fast dynamic control of the M-S4T due to its low-inertia nature. To verify the MPPS, a simulation platform is required. HIL can accelerate the simulation and evaluate the impacts of non-idealities of the controller. Although significant work has been done for HIL simulation of VSCs, there is very little knowledge about HIL simulation for CSCs with small energy storage element using fast dynamic control.

Table 2.4: Summary of the state-of-the-art HIL simulations

References	[82]	[83]	[84]	[85, 86]	[87]	[88]
Topology	two-level inverter	two-level inverter	two-level inverter	MMC with 200 submodules	MMC with 50 submodules	M2DC with 6 HVSM and LVSM
Control algorithm			PI	MPC	PI	PI
System scale	Small	Small	Small	Large	Large	Medium
PHIL/CHIL	CHIL	CHIL	CHIL	CHIL	CHIL	CHIL
Controller implementation			Customized	OPAL-RT	Customized	Customized
Switching frequency	2 kHz	4 kHz	2 kHz	0.3 kHz		10 kHz
Communication time-step (CPU)	50 μs	25 μs		25 μs		
Calculation time-step (FPGA)	0.1 μs	0.5 μs	20 μs	0.5 μs		3μs

CHAPTER 3

M-S4T FOR TRACTION APPLICATIONS

3.1 Single-phase AC to DC Configuration

The circuit diagram of the traction converter based on the M-S4T is shown in Fig. 3.1. The basics of operation of the converter is the same as discussed in Chapter 2 and shown in Fig. 3.2. Due to the modular configuration of the M-S4T, the operation of each module is symmetrical. In the converter of Fig. 3.1, the input port charges L_m while the output port discharges L_m. Therefore, the volt-second balance of L_m is maintained. The input bridge

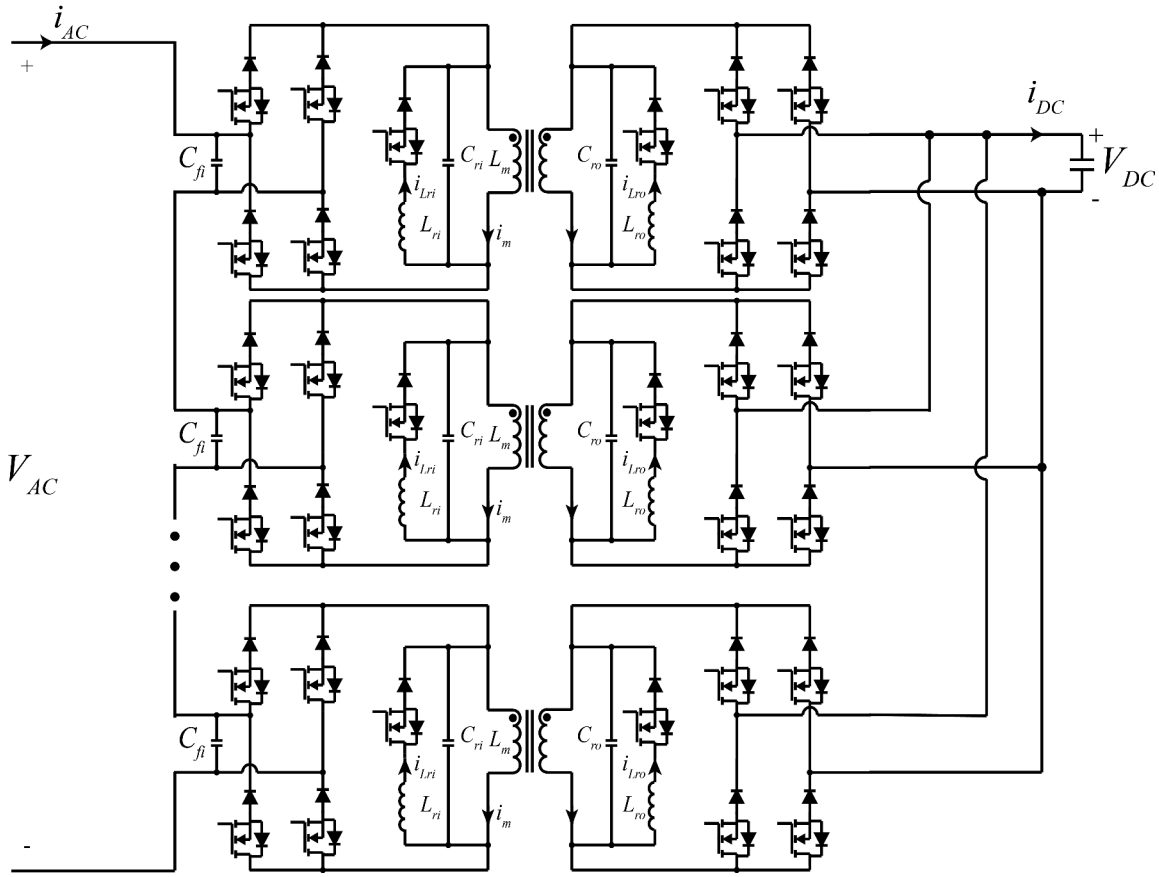


Figure 3.1: Circuit diagram of the AC-DC configuration of the M-S4T for traction applications.

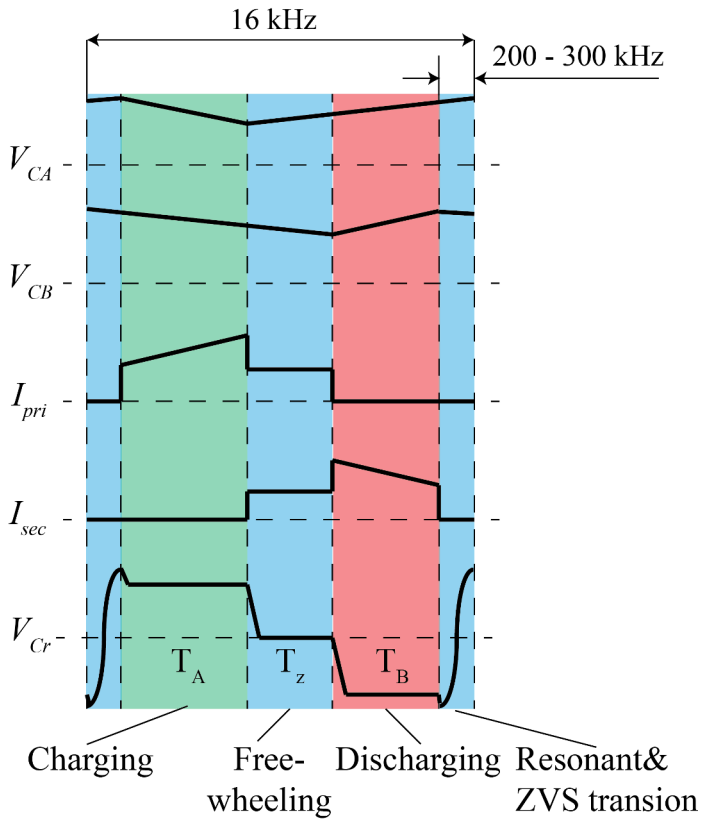


Figure 3.2: Operating principle of S4T [20].

duty cycle is varying depending on the sinusoidal input voltage. The input power of the single phase AC grid at unity power factor is calculated as:

$$P_{AC} = P_{DC} + P_{DC}sin(2\omega t). \tag{3.1}$$

where ω is the grid frequency. As shown in (3.1), the double-line-frequency (DLF) pulsating power needs to be buffered by the DC-side capacitor. The required DC-side capacitance is calculated as:

$$C_{buffer,DC} = \frac{P_{DC}}{2\omega V_{DC}\Delta v}. \tag{3.2}$$

where Δv is the allowed ripple on the DC side. In this configuration, since both the DC and ripple components of the buffer capacitor voltage are required to meet the specification of the following motor drive, selection of the capacitance value is not flexible.

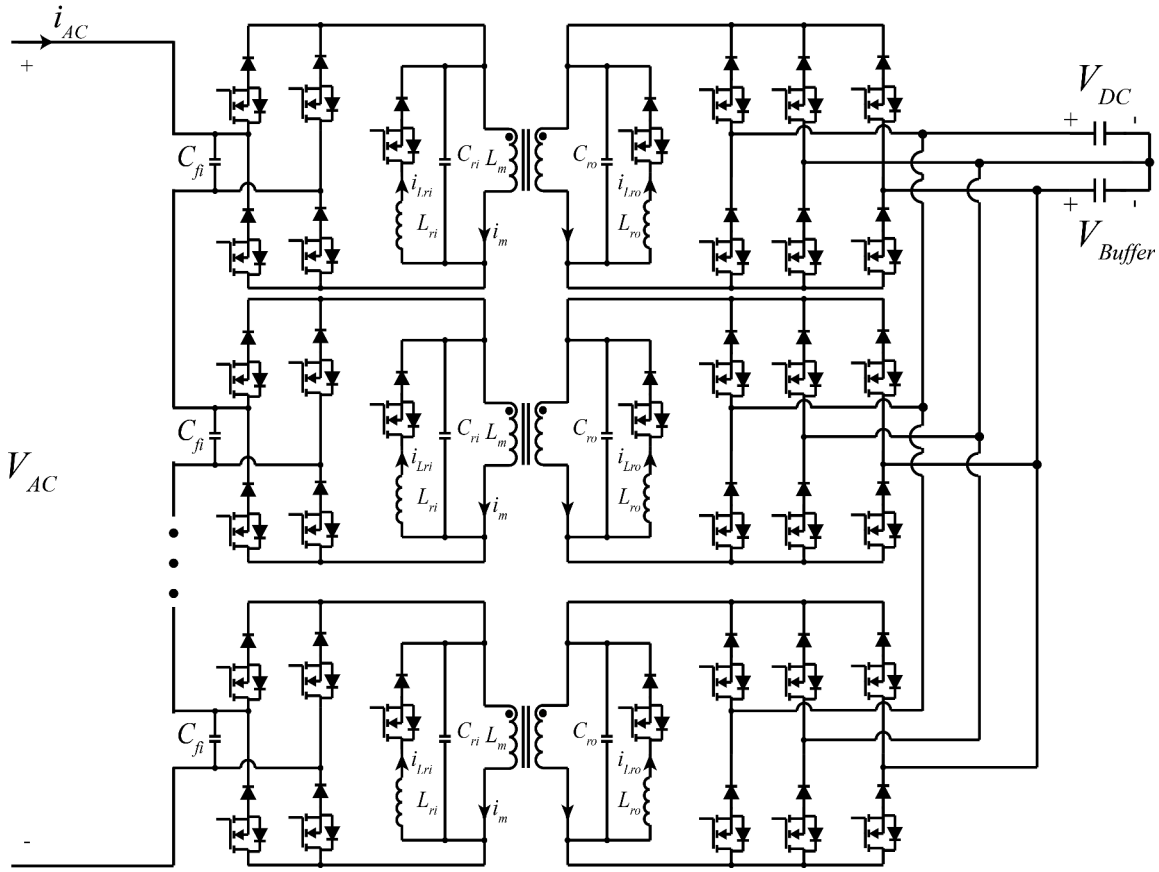


Figure 3.3: Circuit diagram of the AC-DC configuration of the M-S4T with buffer capacitor.

3.2 Single-phase AC to DC Configuration with DC Buffer Capacitor

Another configuration of the M-S4T for single-phase AC applications is shown in Fig. 3.3. Compared to the configuration shown in Fig. 3.1, Fig. 3.3 adds another leg on the output bridge of the converter. The additional leg connects a buffer capacitor to the converter to absorb the DLF pulsating power. The required capacitance is calculated by (3.2). Compared to the configuration in Fig. 3.1, in this configuration, both the DC and ripple components of the buffer capacitor voltage are not fixed. Therefore, selection of capacitance is more flexible compared to Fig. 3.1.

The operation of this configuration is more complex because of the additional leg. The AC input port and DC output port are the same compared to the previous configuration.

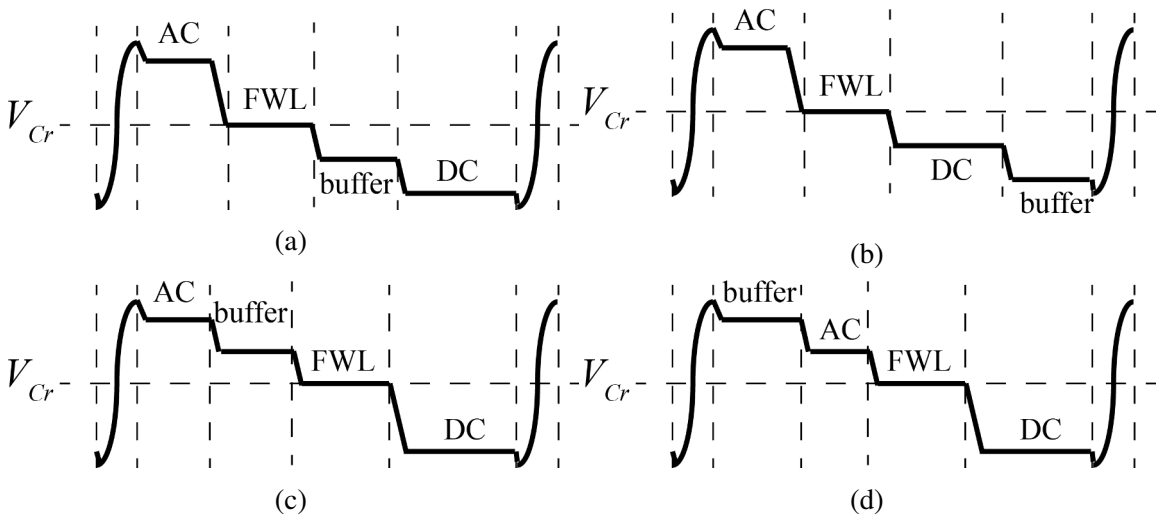


Figure 3.4: Resonant capacitor voltage for (a) discharging, $V_{DC} > V_{buffer}$, (b) discharging, $V_{DC} < V_{buffer}$, (c) charging, $V_{AC} > V_{buffer}$ and (d) charging, $V_{AC} < V_{buffer}$.

For the additional buffer port, it discharges L_m when P_{AC} is larger than P_{DC} and charges L_m when P_{ac} is smaller than P_{DC}. Depending on the relative magnitude of each port, there are four possible switching sequence in each switching cycle:

- when $P_{AC} > P_{DC}$ and $V_{DC} > V_{buffer}$: the sequence is AC port, buffer port, DC port, as shown in Fig. 3.4(a);
- when $P_{AC} > P_{DC}$ and $V_{DC} < V_{buffer}$: the sequence is AC port, DC port, buffer port, as shown in Fig. 3.4(b);
- when $P_{AC} < P_{DC}$ and $V_{AC} > V_{buffer}$: the sequence is AC port, buffer port, DC port, as shown in Fig. 3.4(c);
- when $P_{AC} < P_{DC}$ and $V_{AC} < V_{buffer}$: the sequence is buffer port, AC port, DC port, as shown in Fig. 3.4(d).

Since the buffer port voltage selection is flexible in this configuration, it can be selected to simplify the sequence.

3.3 Single-phase AC to DC Configuration with AC Buffer Capacitor

The functionality of the buffer port is to absorb the DLF pulsating power, which means the buffer capacitance shown in Fig. 3.3 can operate without maintaining a DC voltage. Therefore, a variant of the configuration in Fig. 3.3 is to use an AC capacitance instead of a DC capacitance. By using an AC capacitance, the required capacitance is calculated by:

$$C_{buffer,AC} = \frac{P_{DC}}{2\omega V_{AC}^2}. \tag{3.3}$$

where V_{AC} is the peak voltage of the AC buffer capacitance. Therefore, if the required peak voltages of the AC and DC capacitances are the same, the AC capacitance is much smaller than the DC one.

However, when using an AC capacitance, the voltage of the AC port is always changing. Therefore, all the four sequences shown in Fig. 3.4 are possible, which add to the controller design complexity.

3.4 Single-phase AC to 3-phase AC Configuration

Another configuration based on the M-S4T is shown in Fig. 3.5. In this configuration, unlike the other configurations, which provide a DC link to a following motor drive, the single-phase AC is directly converted to 3-phase AC to drive the motor directly. Depending on the filter capacitor size, the buffer port similar to the previous configurations can be added. The motor drive capability of the S4T is already shown in [91]. However, by using this topology, the auxiliary power supply in the railway vehicle cannot be achieved. Therefore, another converter is required to provide a DC bus for the auxiliary power supply.

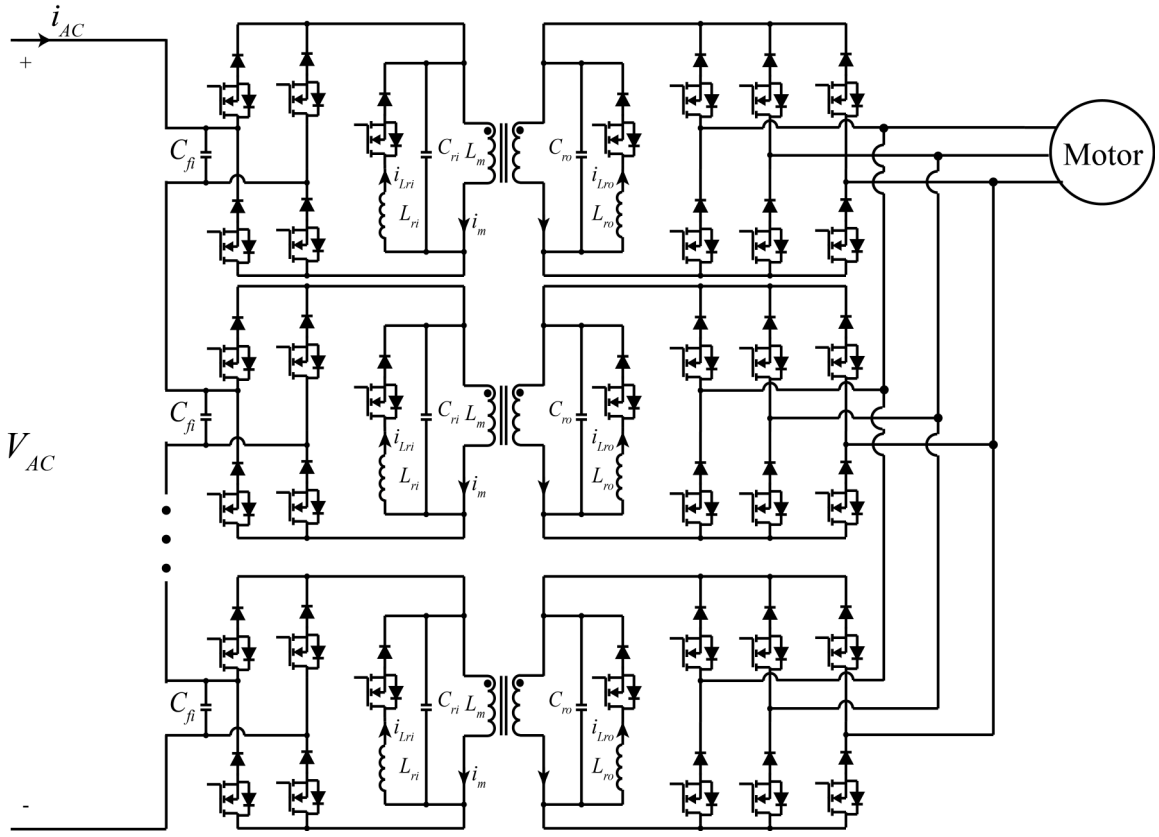


Figure 3.5: Circuit diagram of the converter configuration of the M-S4T for drive applications.

3.5 Conclusions

Based on the discussion in previous chapters, the M-S4T is a promising candidate for the next-generation traction converters. The M-S4T can be configured in different ways. In this chapter, all of the configuration options were reviewed and discussed. It is shown that the single-phase AC to DC configuration with DC buffer capacitor is more flexible with less control complexity compared to the other configurations. Therefore, within the rest of the dissertation, the discussion will be focused on this configuration.

CHAPTER 4

SOFT-SWITCHING CHARACTERIZATION OF RB SIC DEVICES

SiC devices rated at >3.3 kV and 50-200 A can simplify the design of MV and HV converters. However, simple drop-in replacement of Si devices with SiC ones can result in issues such as EMI caused by large dv/dt (30-50 kV/μs). However, the use of RB-devices is contingent on deep understanding of the switching transients of devices under soft-switching conditions. In addition, to exploit full benefits of the S4T, practical integration issues of the RB-devices in terms of gating sequences need to be explored and resolved prior to using them.

4.1 Proposed Double Pulse Test Circuit for Soft-switching Characterization

As discussed in Chapter 2, the information on soft-switching characterization of RB-devices is not available. As shown in Fig. 4.1, each RB module is comprised of a series-connected pair of a MOSFET and a diode. Hereinafter, the MOSFET of i$^{\text{th}}$ RB-module (S_i) is called M_i and the diode is called D_i. To characterize the RB module performance in the S4T circuit under soft-switching conditions, a novel DPT circuit is proposed, whose schematic is shown in Fig. 4.2. Compared to Fig. 4.1, the DPT circuit is a simplified circuit of the S4T. The two RB modules (S_{APi}, S_{BNi}) used for charging L_m are reduced to one RB module (S_u) while the other switch pair (S_{APo}, S_{BNo}) used for discharging L_m are reduced to one (S_l). The two resonant circuits comprised of resonant capacitors (C_{ri}, C_{ro}), resonant inductors (L_{ri}, L_{ro}) and resonant switches (S_{ri}, S_{ro}) on both sides of the HF transformer are reduced to one resonant circuit (C_r, L_r, S_r). The HF transformer with a relatively low magnetizing inductance (L_m) is simplified to an inductor (L). The current through L_m (I_m) is replaced by the inductor current (I_L). Compared to the conventional DPT circuits, the proposed circuit can be easily configured to characterize the RB-switches under either

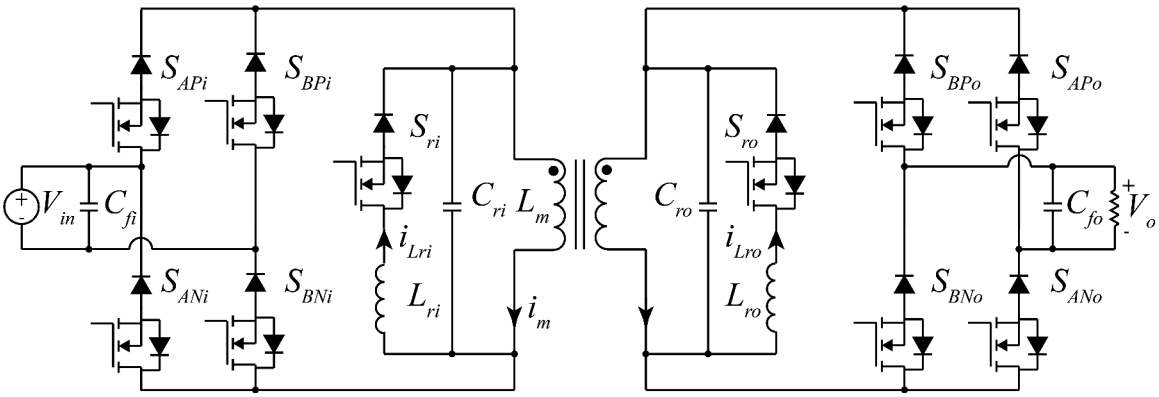


Figure 4.1: Circuit diagram of the S4T for DC-DC applications.

soft-switching or hard-switching conditions by adding or removing the resonant circuit as shown in Fig. 4.2.

4.2 Operation Principle of the Proposed Double Pulse Test Circuit

Operation of the proposed DPT is similar to that of a flyback converter, as is the case with the S4T. As shown in Fig. 4.3(a), under hard-switching condition, when the gate of S_u (GS_u) is high, the DPT operates in charging mode (mode 1) where V_{dc1} charges L and inductor current (i_L) flows through S_u. When the gate of S_l (GS_l) is high and GS_u is low, the DPT operates in discharging mode (mode 2) where V_{dc2} discharges L and i_L flows through S_l. Fig. 4.3(b) illustrates the operation of the circuit under soft-switching condition. Under soft-switching conditions, the voltage of C_r (V_{Cr}) in the DPT needs to be initialized. Before S_u is turned on, C_r is pre-charged to V_{dc1} using an initialization circuit comprised of $SW_{precharge}$, $R_{precharging}$ and S_L as shown in Fig. 4.4 to ensure soft-switching for the first pulse. For subsequent pulses, soft switching can be achieved using the resonant circuit. At t_0, the mechanical relay $SW_{precharge}$ turns on and C_r is charged to V_{dc1} through $R_{precharge}$. Then, S_u is turned on with zero voltage at t_1 with no inrush current flowing through S_u. Subsequent to the completion of pre-charging, $SW_{precharge}$ is turned off at t_2. During these subintervals and switching transitions, i_L needs to be maintained at zero before initialization

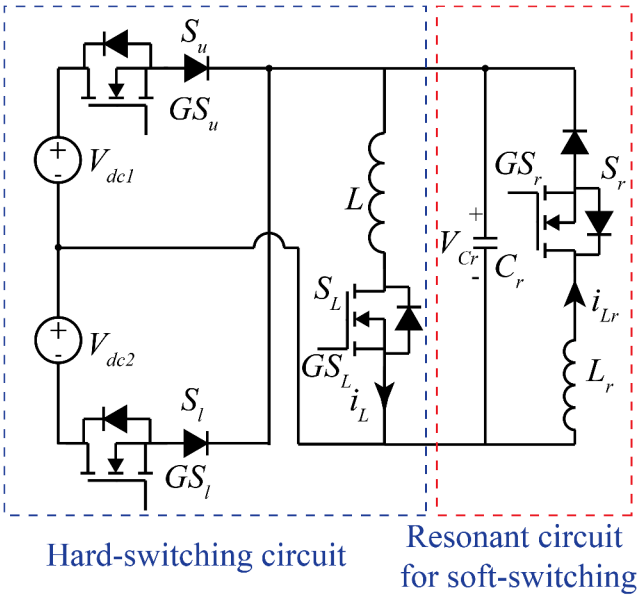


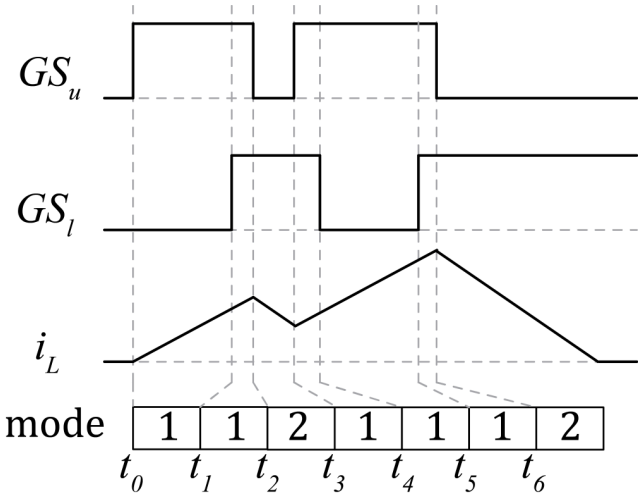
Figure 4.2: Schematic of the proposed DPT circuit.

is done. Therefore, switch S_L is used, which is turned on after $SW_{precharge}$ is turned off. The initialization completes before t_3. At t_3, when S_L is turned on, the DPT operates in mode 1. Once mode 1 ends at t_5 when S_u turns off, the DPT enters ZVS mode (mode -1) to ensure ZVS turn-off of S_u and ZVS turn-on of S_l. In this mode, since C_r is effectively in parallel with the parasitic capacitors of S_u and S_l, the voltage of S_u (V_{Su}) is charged slowly by i_L and V_{Su} increases negligibly while its current drops to zero. Meanwhile, although GS_l is high at t_5, S_l cannot conduct i_L until V_{Cr} is discharged by i_L to $-V_{dc2}$ at t_6 when the voltage of S_l (V_{Sl}) becomes zero and i_L starts flowing through S_l. Therefore, both S_l and S_u are switched on/off with ZVS at this moment. The DPT operates in mode 2 from t_6 to t_7 and in mode -1 after t_7. S_l is turned off in the same manner as S_u. The second pulse starts at t_8. At the beginning of the second pulse, the DPT enters mode 3 in which the negative V_{Cr} is flipped to a positive V_{Cr} higher than V_{dc1} by the resonant circuit. GS_u is turned high once mode 3 ends. Mode 3 is followed by mode -1 in which V_{Cr} is discharged by i_L to V_{dc1} and ZVS turn-on of S_u is achieved. The rest of the second pulse is the same as the aforementioned discussion. At the end of the second pulse, S_u is turned off and S_l is turned on. Therefore,

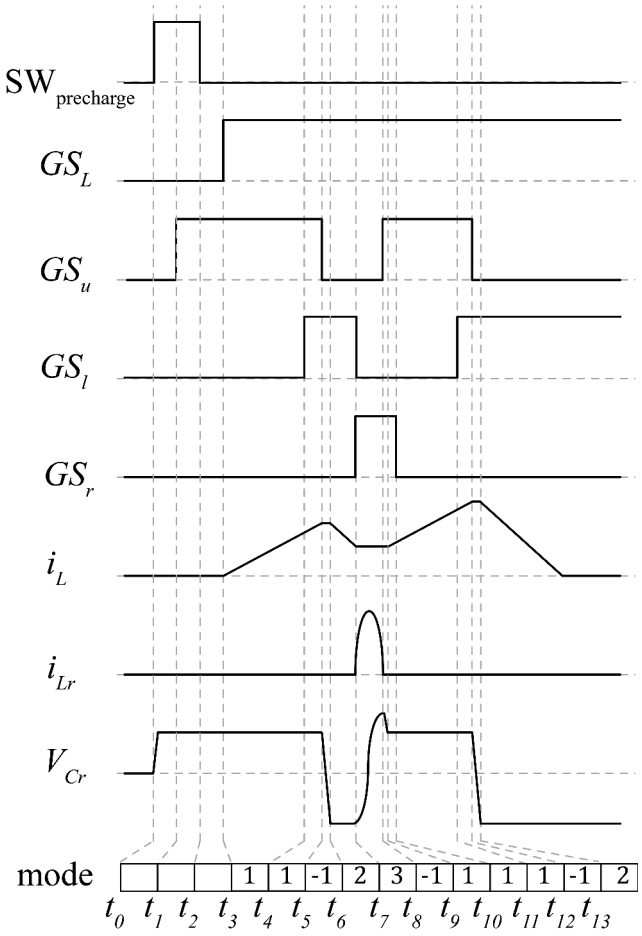
-V_{dc2} is applied to L and inductor current is discharged to 0.

4.3 Experimental Setup

Fig. 4.4 shows the circuit diagram of the experimental setup. S_u is the device under test (DUT). Voltage and current probes are placed to measure V_{RB} and I_{RB} of the DUT, as shown in Fig. 4.4. Fig. 4.5(a) shows a custom 3.3 kV RB SiC module developed by Wolfspeed. The module consists of five identical RB switches with each switch consisting of one 3.3 kV SiC MOSFET and one 3.3 kV SiC diode connected in series. Fig. 4.5(b) shows a custom 1.7 kV RB SiC module using discrete devices in which a 1.7 kV discrete RB-module is realized by using a discrete 1.7 kV SiC MOSFET in series with a discrete 1.7 kV SiC Schottky diode. The 1.7 kV and 3.3 kV modules are almost the same in terms of their layouts except that the 3.3 kV module has a Kelvin source while 1.7 kV one does not. One of the reasons for using a 1.7 kV module is to have access to the diode and switch interconnection, which is not available in the 3.3 kV module. The diode-switch interconnection point is needed to evaluate the dynamic voltage sharing between the diode and the switch. Fig. 4.5(c) shows the internal connection of the 1.7 kV and 3.3 kV modules. Three of the five switches are used in the DPT. Fig. 4.5(d) shows the photo of the experimental setup. By connecting/disconnecting the resonant circuit, the setup can be easily configured for hard-switching or soft-switching characterization. To suppress the current overshoot under hard switching that also exist in the traditional DPT [92] and to protect the device, a ferrite bead is added as shown in Fig. 4.4. The bead is also installed under soft-switching conditions to have a fair comparison of the switching performances. The power stage is designed as shown in Fig. 4.4. The overall test setup is designed to characterize the 3.3 kV RB modules at 2 kV, 25 A condition. In the setup, the core of the inductor L is grounded. The main components used in the DPT are listed in Table 4.1.



(a)



(b)

Figure 4.3: (a) conceptual waveforms under hard-switching; and (b) conceptual waveforms under soft-switching.

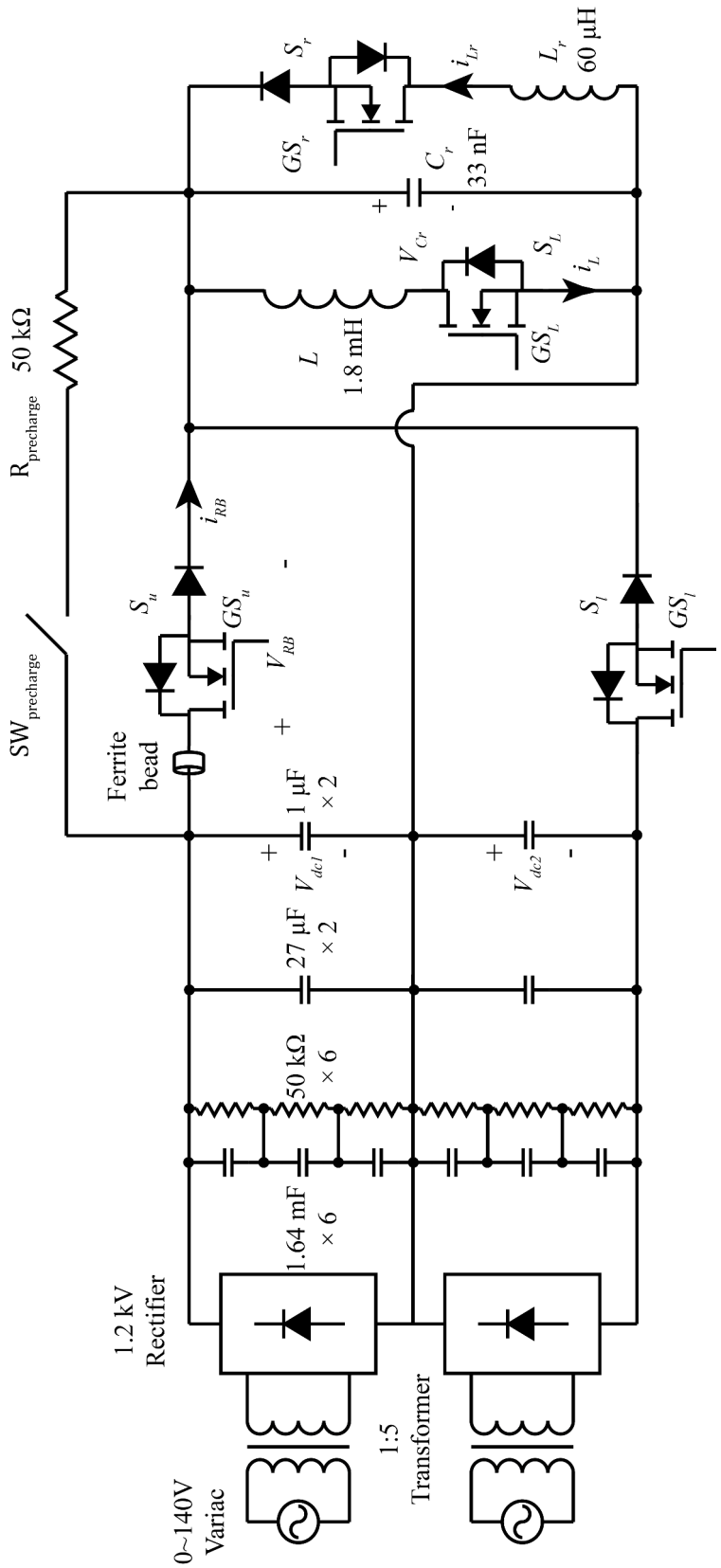
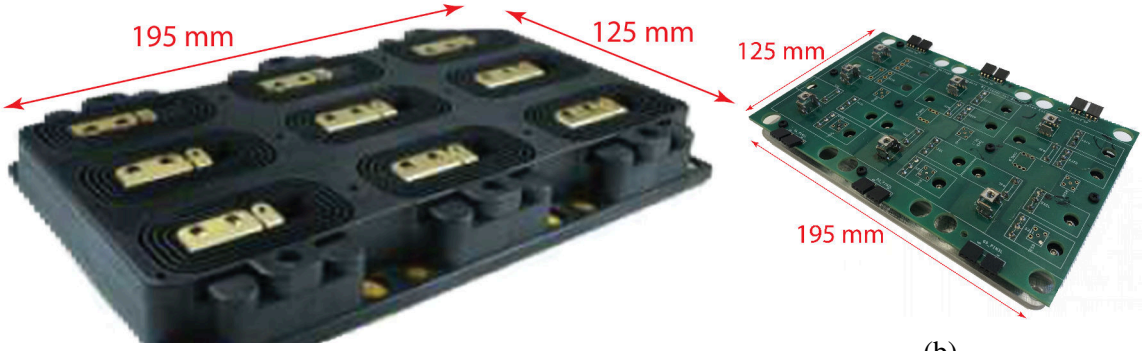
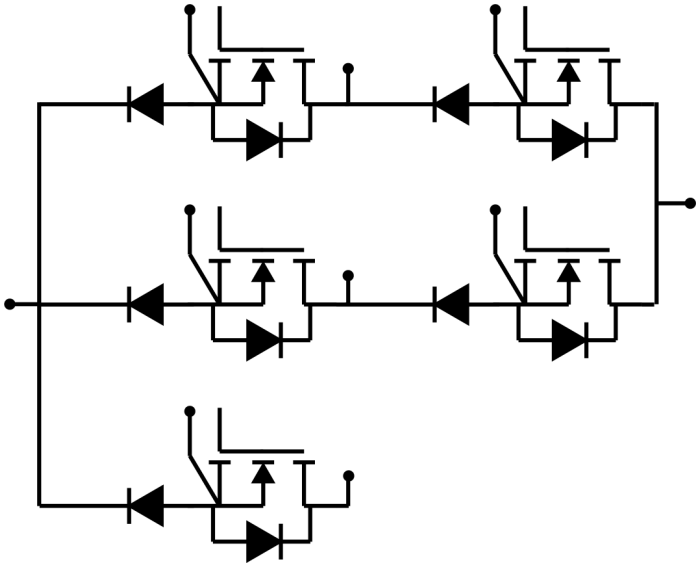


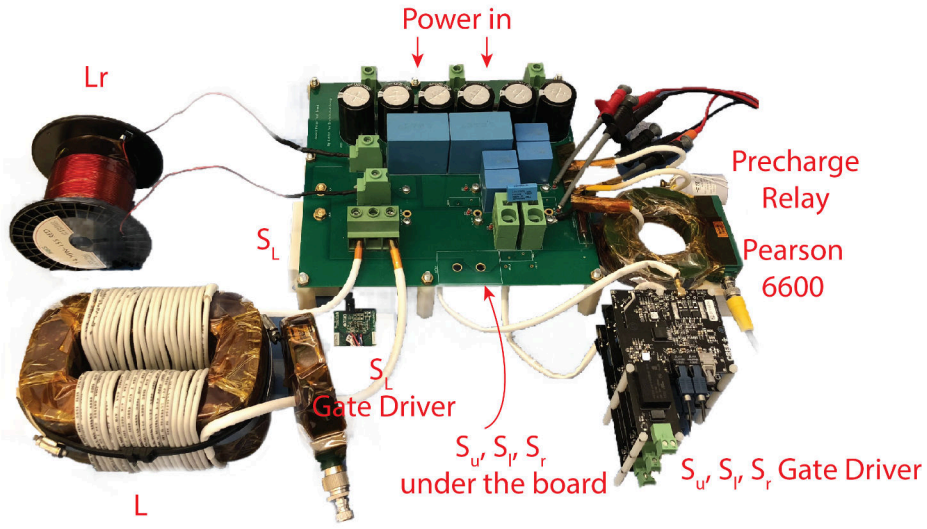
Figure 4.4: Circuit diagram of the experimental setup for the DPT.



(a) (b)



(c)



(d)

Figure 4.5: (a) 3.3 kV, 45A Wolfspeed RB-device module; (b) 1.7 kV, 10A module; (c) schematic of the modules; (d) image of the 2kV, 25A DPT.

Table 4.1: Main Component of the DPT

Element	Description
RB module	3.3 kV, 45A Wolfspeed module Or 1.7 kV, 10A module Wolfspeed C2M1000170DGeneSiCGB10MPS17
RB module Gate Driver	3.3 kV Wolfspeed Gate Driver Or1.7 kV Wolfspeed CRD-001
L	1.8 mH
L_r	60 μH
C_r	33 nF KEMET CKC33C223KJGACTU
Voltage Probe	Teledyne Lecroy HVD3605 BW=100MHz
Current Probe	Pearson 6600 BW=120MHz

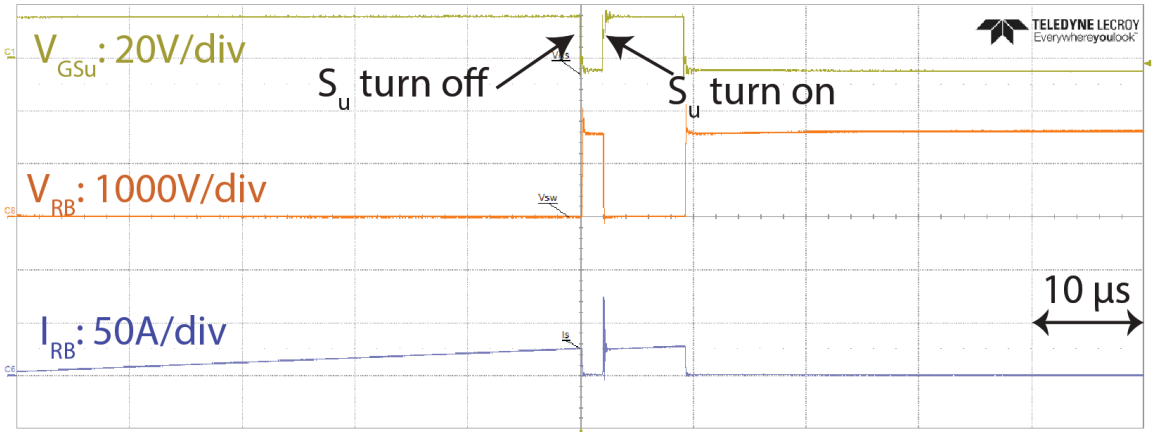
4.4 Experimental Waveforms

The waveforms for both hard and soft switching at 1.6 kV 25 A are shown in Figs. 4.6(a) and 4.7(a), respectively. Figs. 4.6(b) and 4.6(c) and Figs. 4.7(b) and 4.7(c) illustrate the magnified portions of the hard-switching and soft-switching waveforms during turn-on and turn-off switching transitions. Delay in the I_{RB} probe compared to voltage probe is 15 ns and is compensated in loss calculation. Due to the resonant circuit, the DUT is turned on with zero voltage across it, thus the turn-on loss is zero. The turn-off loss depends on the value of dv/dt , which can be controlled by appropriate selection of C_r. In this test, C_r is chosen to achieve a dv/dt of 0.6 kV/μs compared to 25-30 kV/μs under hard-switching condition.

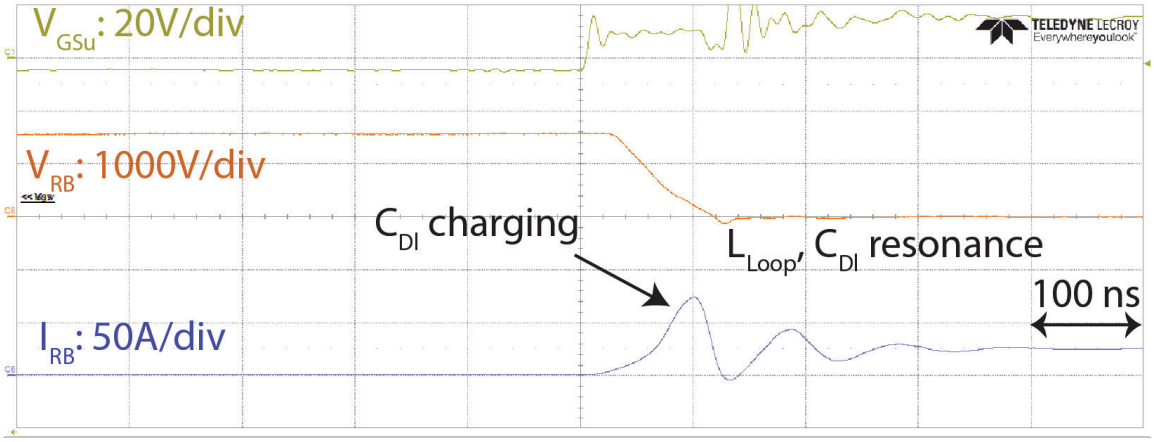
4.5 Power Losses

The main switching modules (S_u and S_l) are characterized under different voltage and current levels up to 2 kV, 25 A. Turn-on and turn-off losses are calculated by:

$$E_{on} = \int_{10\%\ of\ I_{L,pk}}^{90\%\ of\ I_{L,pk}} V_{RB} \cdot I_{RB}\, dt, \tag{4.1a}$$



(a)



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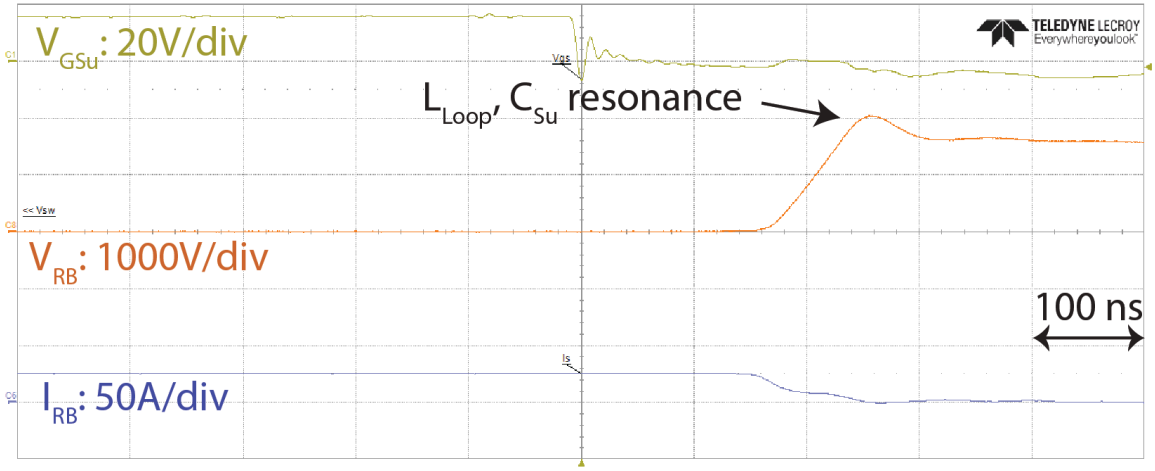
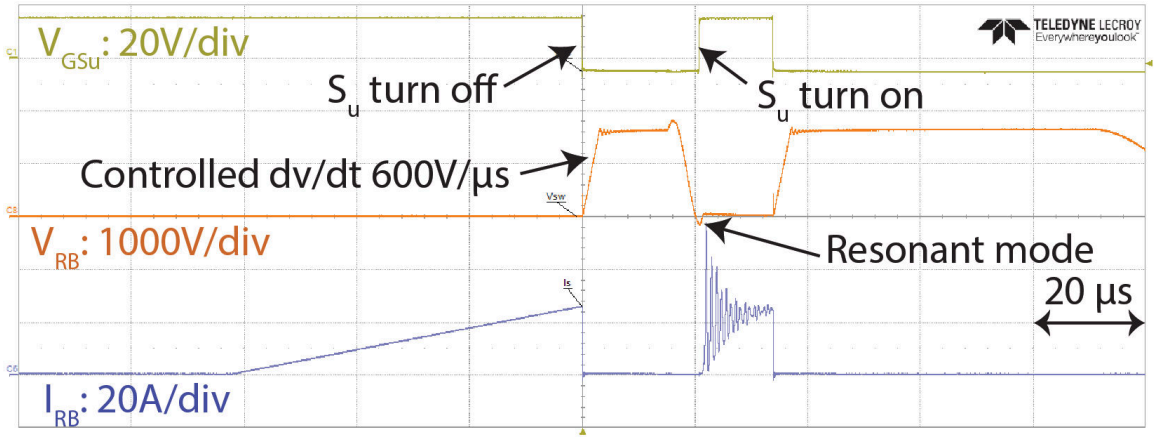
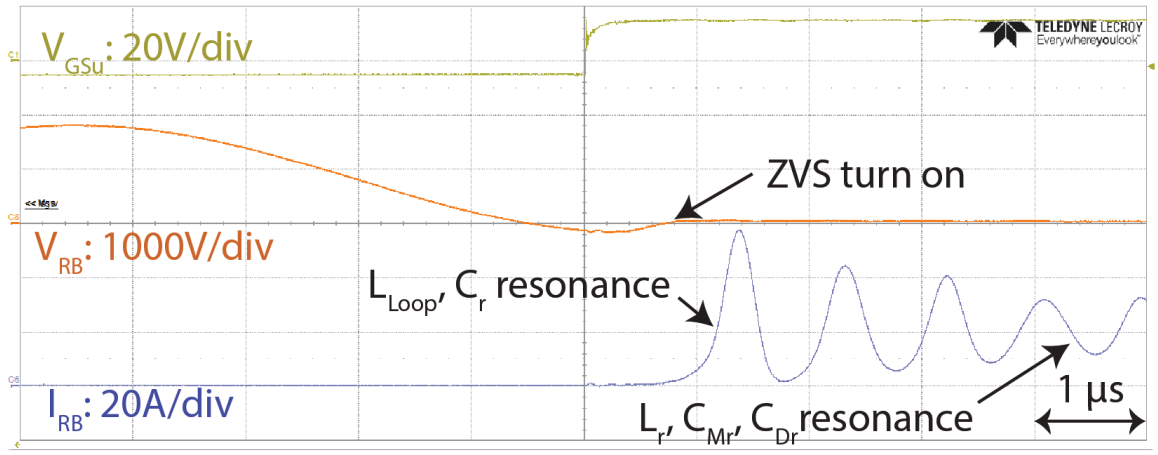


(c)

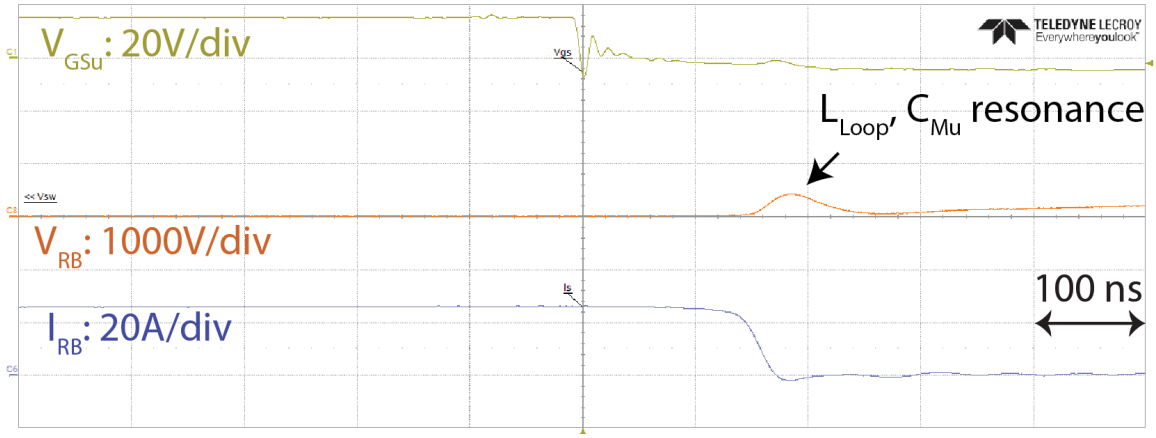
Figure 4.6: Experimental results of hard-switching at 1.6 kV, 25A (a) overall voltage and current waveforms, and (b,c) turn-on and turn-off switching transients, respectively.



(a)



(b)



(c)

Figure 4.7: Experimental results of soft-switching at 1.6 kV, 25A (a) overall voltage and current waveforms, and (b,c) turn-on and turn-off switching transients, respectively.

$$E_{off} = \int_{90\%\ of\ I_{L,pk}}^{10\%\ of\ I_{L,pk}} V_{RB} \cdot I_{RB}\, dt, \tag{4.1b}$$

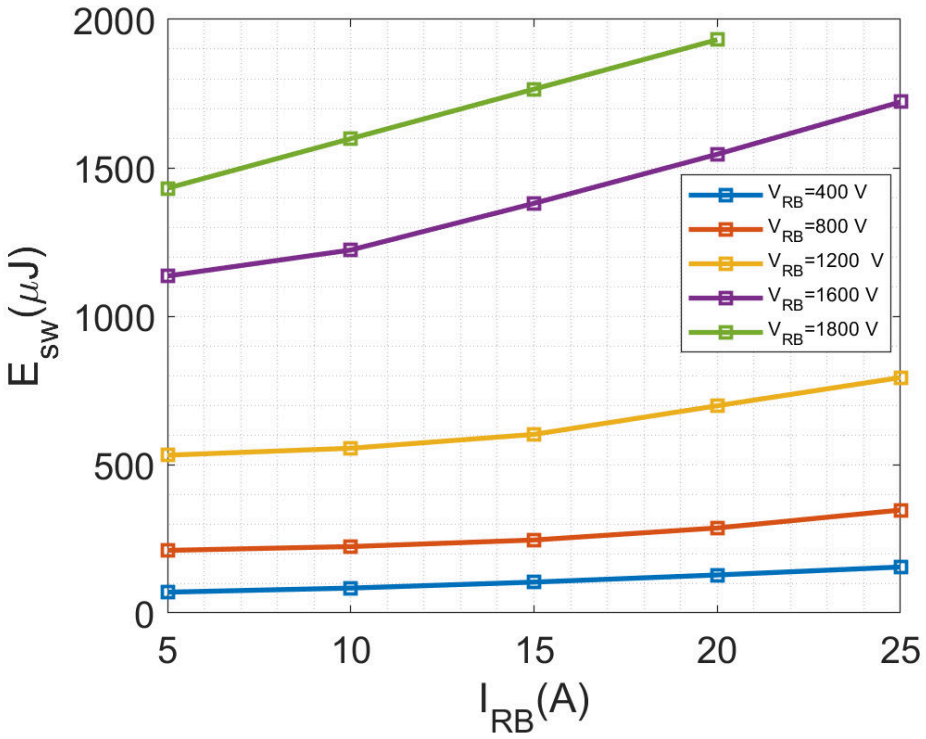
$$E_{sw} = E_{on} + E_{off}. \tag{4.1c}$$

Since S_u turns on when its voltage is zero, E_{on} is zero and soft-switching losses only include the turn-off losses. The losses during turn-off transition are comprised of device losses and energy stored in the parasitic loop inductance (L_{loop}), which is dissipated in the loop resistance. At 1.6 kV, 25 A, the total turn-off losses are 26.9 μJ, of which 3.7 μJ is due to the device characteristic while the remaining 23.2 μJ due to the energy trapped in the L_{loop}. Compared to the device losses, L_{loop} energy dominates the turn-off losses, which is discussed in the following section. Device losses are dependent on the value of dv/dt selected, which is 0.6 kV/μs in this case. Fig. 4.8 shows the total switching losses E_{sw} under different voltage and current levels for both hard switching and soft switching. As compared to hard switching, soft switching shows significant power loss reduction in the main switching modules, i.e., 98.5$\%$, as shown in Fig. 4.8.

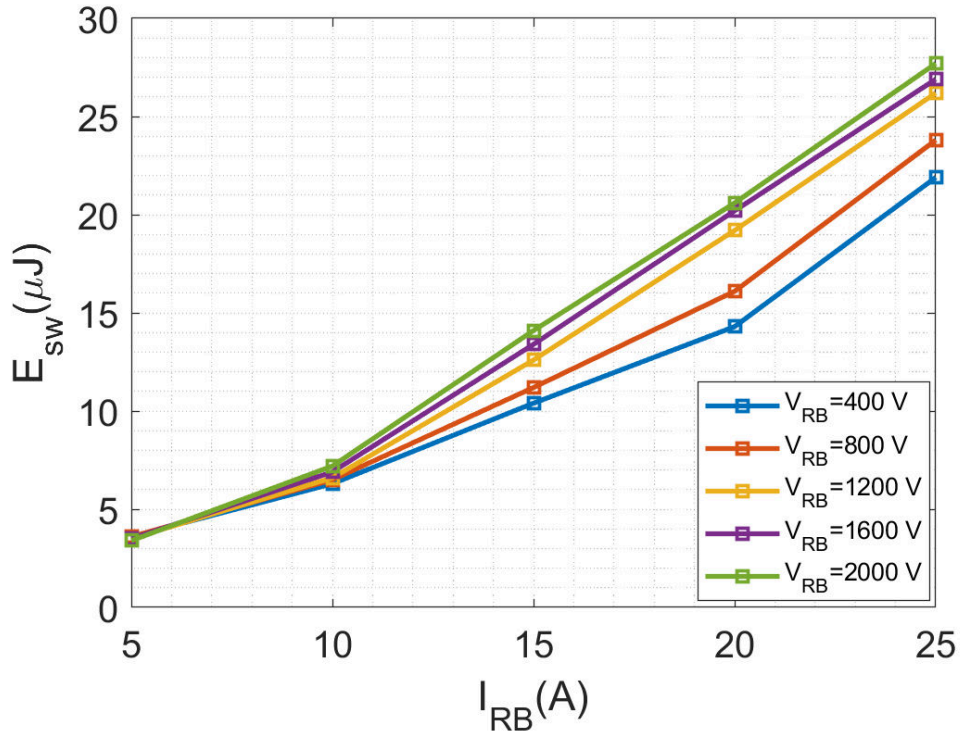
It is noticeable that the resonant RB module S_r is turned on and off at ZCS because of presence of L_r, which limits the di/dt and its reverse blocking characteristic. However, when S_r is turned on, M_r is blocking V_{Cr} and the capacitive energy associated with the device parasitic capacitor appears as the switching loss of S_r. This portion of energy is lost internally in the device and cannot be measured (the current does not appear at the terminals). At 2 kV, the device output capacitance is 50 pF and this energy is estimated to be 100 μJ, which equals to $\frac{1}{2}CV_{Cr}^2$.

4.6 Current and Voltage Stresses

As shown in Figs. 4.6 and 4.7, under hard switching, the maximum device voltage and current stresses are 2 kV and 75 A, respectively, while under soft switching, those stresses



(a)



(b)

Figure 4.8: Power loss comparison of 3.3 kV RB-device (a) hard-switching losses and (b) soft-switching losses.

Table 4.2: Comparison between hard-switching and soft-switching conditions at 1.6 kV, 25A using 3.3 kV SiC RB module

	Hard-switching	Soft-switching
Total Switching losses (μJ)	1722	26.9
dv/dt (kV/μs)	25	0.6
di/dt (A/μs)	500	550
S_u voltage stress (kV)	2	1.8
S_u current stress (A)	75	56
S_u gate voltage stress (V)	20	16

are 1.8 kV and 56 A, respectively. It is also noticed that the maximum gate voltage stress is larger than 20 V under hard-switching condition compared to 15 V under soft-switching condition. Table 4.2 summarizes a comparison between hard-switching and soft-switching conditions at 1.6 kV, 25A.

4.7 Resonance Caused by Parasitics

As observed in Figs. 4.6 and 4.7, resonance occurs at the instant when the devices are switched. Like the conventional DPT, L_{loop} and device capacitance cause these unwanted resonances. The various parasitic elements causing these resonances are identified and labeled in Figs. 4.6 and 4.7. By observing the resonant frequency in Figs. 4.6 and 4.7, L_{loop} that is comprised of devices internal inductance (L_{device}), wiring inductance (L_{wire}) and equivalent series inductance (ESL) of the DC bus capacitance, is estimated as labeled in Fig. 4.9.

It is noticeable that when the device is turning off, a voltage bump appears on the device voltage as shown in Fig. 4.7(c). The energy trapped in L_{loop} before turn-off is transferred to the capacitance of S_u at this instant and is appeared as a part of the turn-off losses when using V-I integration. Therefore, lower L_{loop} will decrease L_{loop} energy, which will decrease the total switching losses consequently. Fig. 4.7(b) shows a significant resonance in the device current after the resonant mode when S_u turns on. The equivalent circuit of this instant is shown in Fig. 4.10. When S_r turns off and S_u turns on, two resonances occur at

the same time. If there is any energy left in L_r, it will trigger the first resonance between L_r and C_{Mr} and C_{Dr}. On the other hand, a second resonance between L_{loop} and C_r occurs at the same time. Considering the value of L_r, C_{Mr}, C_{Dr}, L_{loop} and C_r, the critical damping resistance for the two resonances can be calculated by:

$$R_1 = 2\sqrt{\frac{L_r}{C_{Mr}//C_{Dr}}}, \tag{4.2a}$$

$$R_2 = 2\sqrt{\frac{L_{loop}}{C_r}}. \tag{4.2b}$$

$R_{damp,1}$ is much larger than $R_{damp,2}$ which means that the first resonance is harder to be damped compared to the second one. If S_r is properly controlled to switch at zero current, the first resonance (L_r, C_{Mr}, C_{Dr}) can be minimized and the total resonance can be easily damped. Fig. 4.11 shows the turn-off transients of S_r with different initial currents in L_r under 400 V, 5 A test condition.

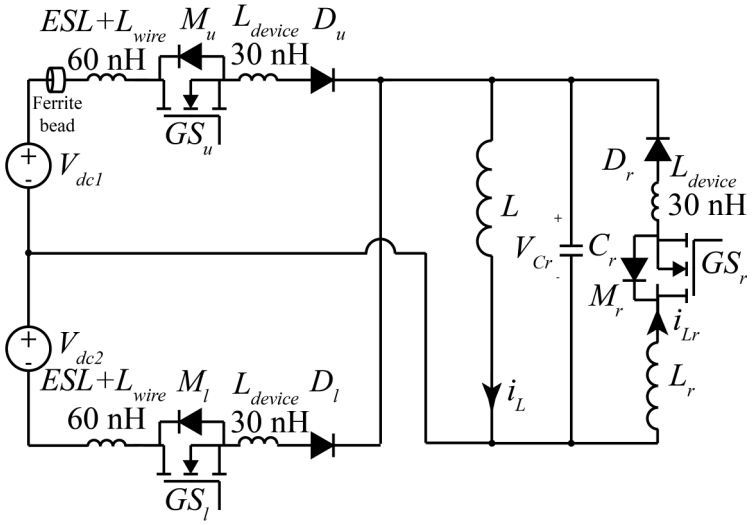


Figure 4.9: Schematic of the DPT including the parasitic inductance.

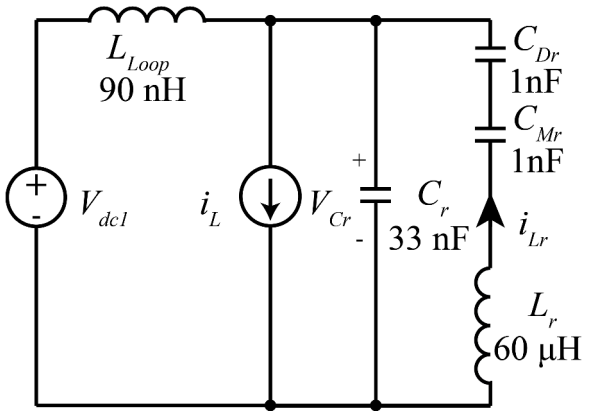
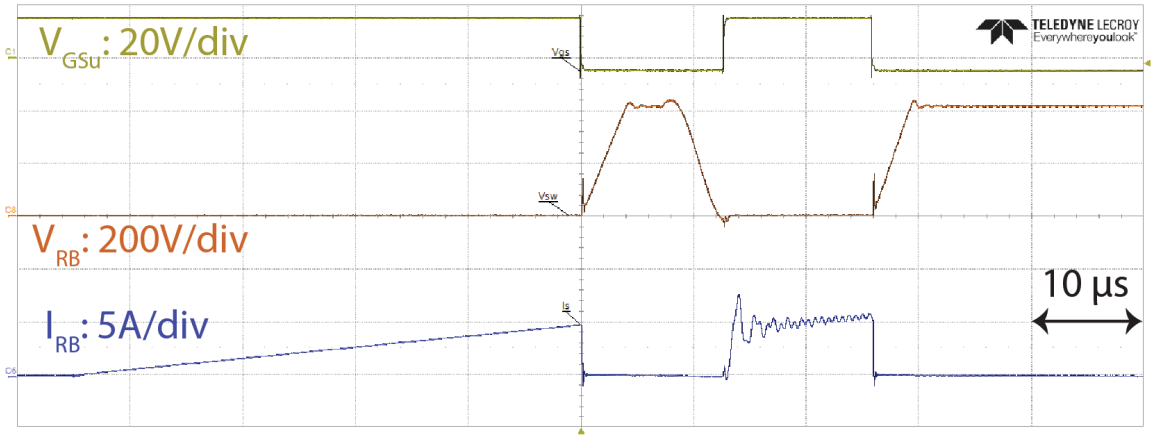
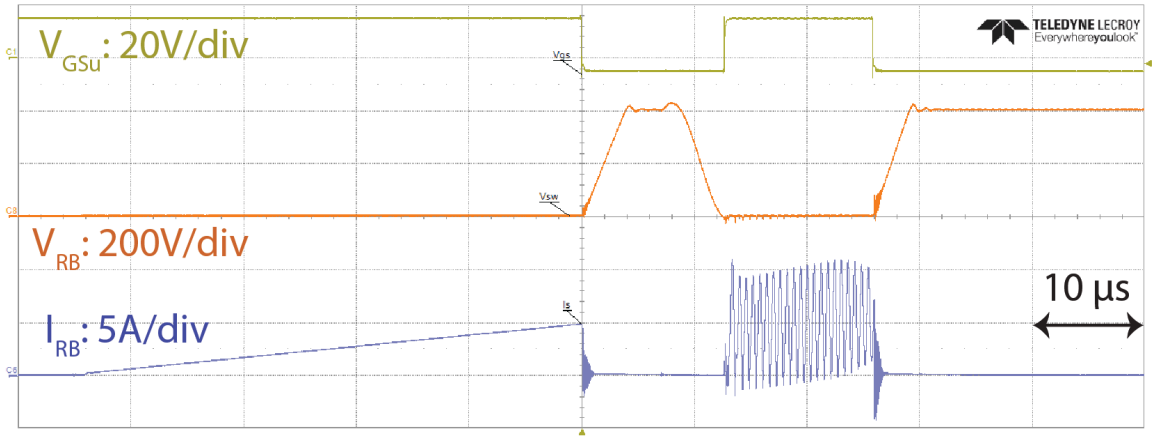


Figure 4.10: Equivalent circuit of turn-on resonance.



(a)



(b)

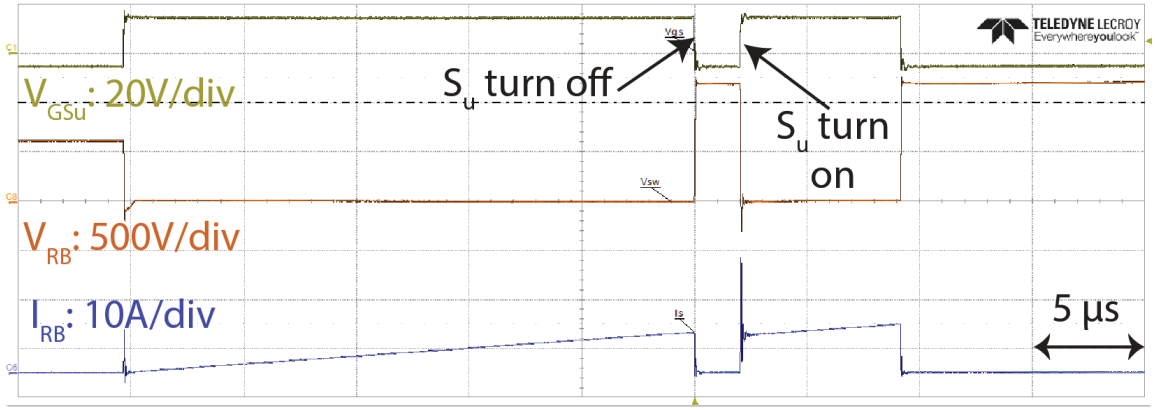
Figure 4.11: Turn-off transient of Sr with (a) low ILr and (b) high ILr.

Table 4.3: Comparison between hard-switching and soft-switching conditions at 1.2 kV, 8A using 1.7 kV SiC RB module

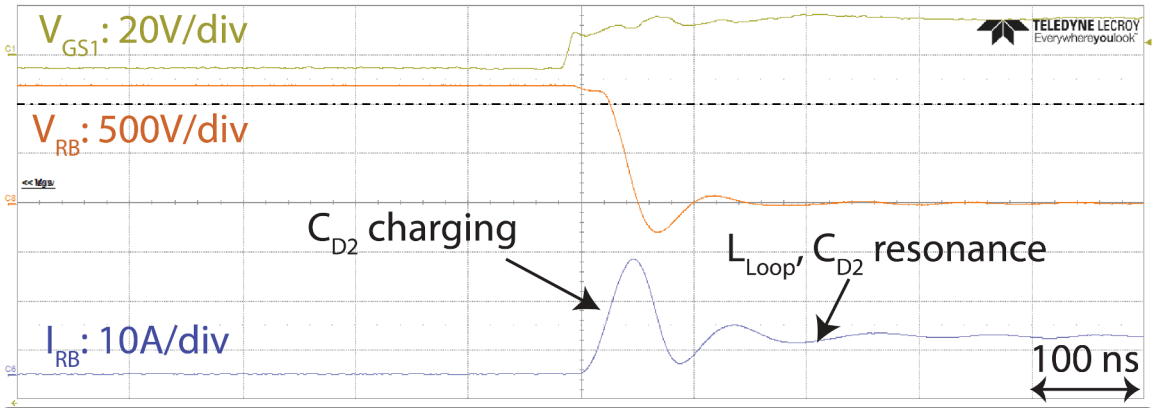
	Hard-switching	Soft-switching
Total Switching losses (μJ)	254.6	3.2
dv/dt (kV/μs)	30	0.5
di/dt (A/μs)	460	490
S_u voltage stress (kV)	1.25	1.3
S_u current stress (A)	24	11
S_u gate voltage stress (V)	18	18

4.8 Characterization of 1.7 kV SiC Reverse-blocking Modules

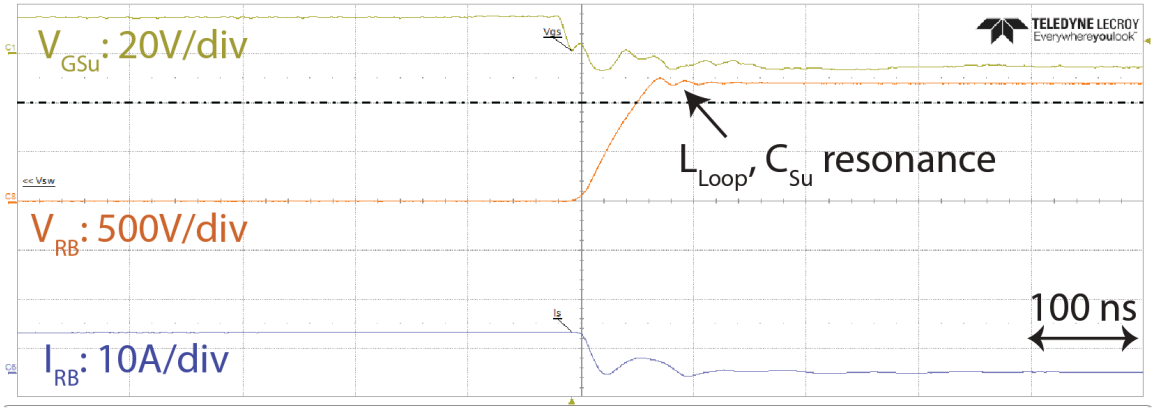
Besides the characterization of 3.3 kV Wolfspeed SiC reverse-blocking module, the custom 1.7 kV SiC reverse-blocking module using discrete devices is characterized using the same test bench and test procedure. The waveforms for both hard switching and soft switching at 1.2 kV 8 A are shown in Figs. 4.12(a) and 4.13(a), respectively. The magnified portions of the hard-switching and soft-switching waveforms during the turn-on and turn-off switching transitions are shown in Figs. 4.12(b) and (c) and Figs. 4.13(b) and (c). Similar to the 3.3 kV RB-module, the turn-on loss of the DUT is zero. In addition, turn-off dv/dt of 0.5 kV/μs is achieved. Compared to the 3.3 kV Wolfspeed SiC RB-module, the custom module has higher internal parasitic inductanc, which is 60 nH calculated by the same method, described in the previous section. Table 4.3 summarizes a comparison between hard-switching and soft-switching conditions at 1.2 kV, 8 A. Similar to the 3.3 kV module, the stresses are less under soft-switching conditions. The di/dt is 490 A/ns when R_g is 5 Ω while it is 180 A/ns when R_g is 25 Ω . The total switching losses E_{sw} under different voltage and current levels up to 1.2 kV, 8 A for both hard switching and soft switching are shown in Fig. 4.14. As compared to hard switching, soft switching shows 98.7$\%$ power loss reduction in the main switching modules, which is similar to the 3.3 kV module.



(a)

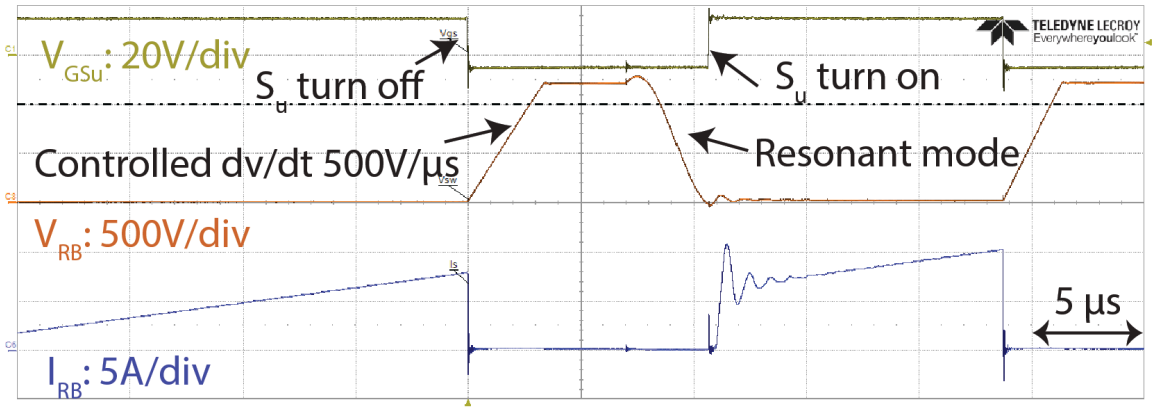


(b)

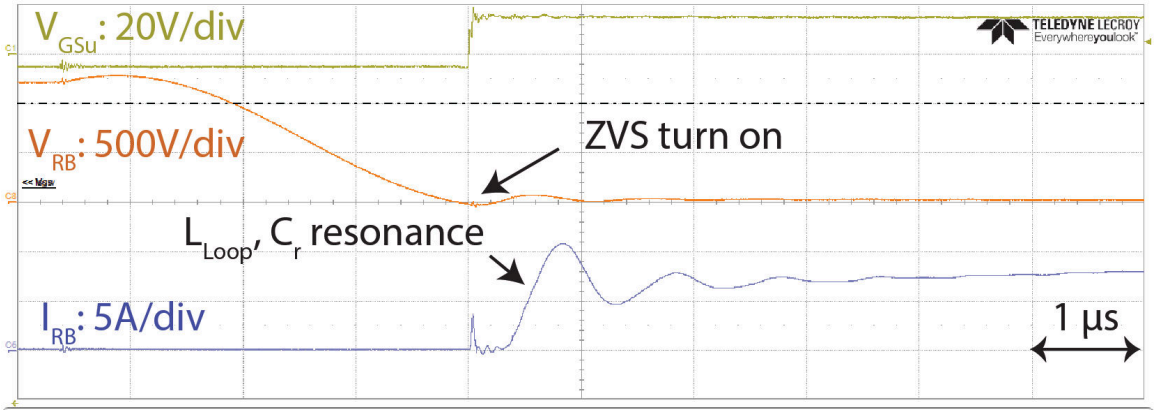


(c)

Figure 4.12: Experimental results of the 1.7 kV SiC RB module under hard-switching at 1.2 kV, 8 A (a) overall voltage and current waveforms, and (b,c) turn-on and turn-off switching transients, respectively.



(a)



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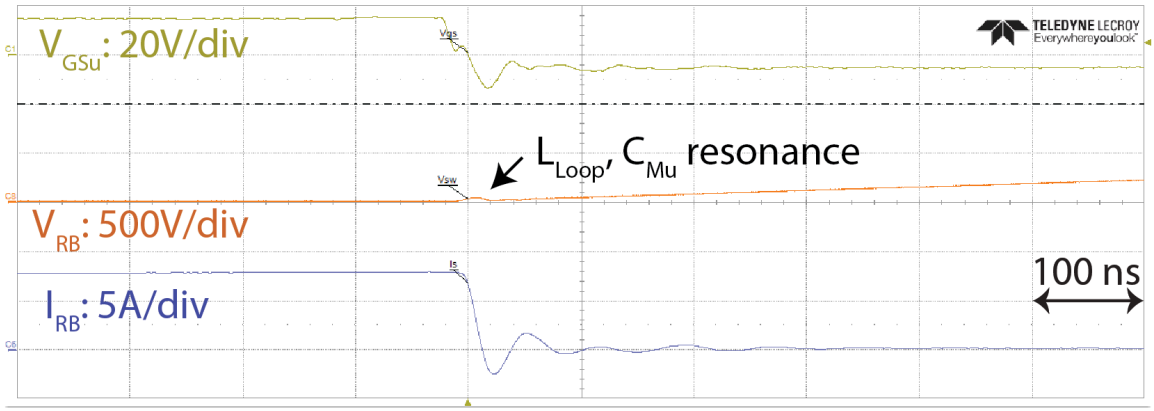
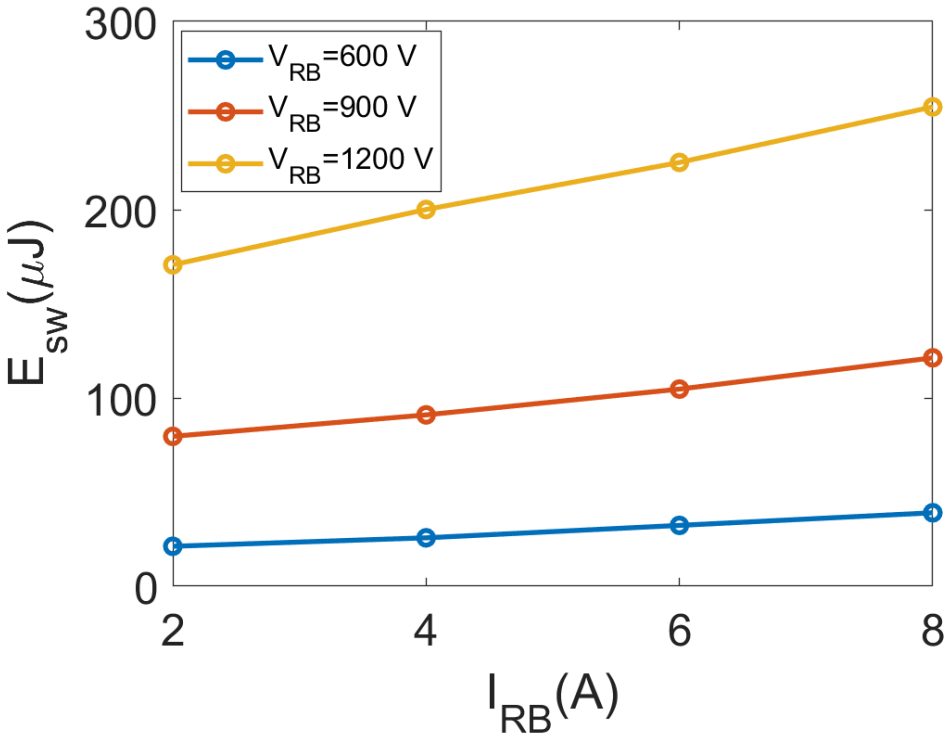
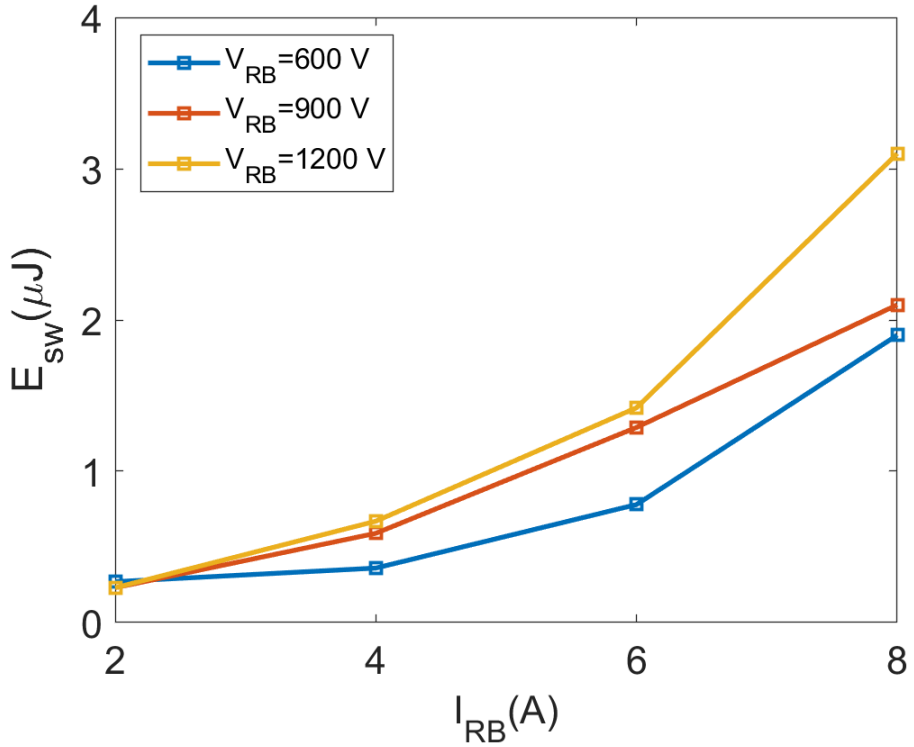


(c)

Figure 4.13: Experimental results of the 1.7 kV SiC RB module under soft-switching at 1.2 kV, 8 A (a) overall voltage and current waveforms, and (b,c) turn-on and turn-off switching transients, respectively.



(a)



(b)

Figure 4.14: Power loss comparison of 1.7 kV RB-device (a) hard-switching losses and (b) soft-switching losses.

4.9 Dynamic Voltage Sharing During Turn-on

The 1.7 kV SiC RB module built based on using discrete switch and diode, enables evaluating the dynamic voltage sharing between the diode and the switch. Although, as shown in Fig. 4.7(b) and Fig. 4.13(b), the total voltage across RB module S_u is zero during turn-on, the voltages across M_u and D_u are not zero. Fig. 4.15(a) shows a turn-on transition of S_u while Fig. 4.16(a) shows the equivalent circuit.

Prior to L_r and C_r resonance:

$$V_{Su} = V_{dc1} + V_{dc2}, \tag{4.3a}$$

$$V_{Du} = 0. \tag{4.3b}$$

During resonance, due to the existence of device capacitors C_{Mu} and C_{Du}, a small portion of the current flows through C_{Mu} and C_{Du}. This current charges C_{Du} and discharges C_{Mu}. Therefore, when the resonant stage ends, as shown in Fig. 4.15(a), V_{Su} is 500 V and V_{Du} is -500 V when the test condition is 1.2 kV and 8 A, indicating that C_{Mu} and C_{Du} both store energy based on:

$$V_{Mu} + V_{Du} = V_{dc1} - V_{Cr}, \tag{4.4a}$$

$$i = -C_{eq}\frac{d\left(V_{Mu} + V_{Du}\right)}{dt} = C_{eq}\frac{dV_{Cr}}{dt}.V_{Cr}\left(0\right) = -V_2, V_{Cr}\left(\infty\right) = V_{dc1} \tag{4.4b}$$

where $C_{eq} = C_{Mu}||C_{Du}$. V_{Du} and V_{Mu} are calculated by:

$$V_{Mu} = V_{Mu}\left(0\right) - \frac{1}{C_{Mu}}\int idt, V_{Mu}\left(0\right) = V_{dc1} + V_{dc2}, \tag{4.5a}$$

$$V_{Mu} = \frac{C_{Mu}}{C_{Mu} + C_{Du}} (V_{dc1} + V_{dc2}) \tag{4.5b}$$

$$V_{Du} = V_{Du}(0) - \frac{1}{C_{Du}} \int i dt, V_{Du}(0) = 0 \tag{4.5c}$$

$$V_{Du} = -\frac{C_{Mu}}{C_{Mu} + C_{Du}} (V_{dc1} + V_{dc2}) \tag{4.5d}$$

Based on (4.5), the values of C_{Mu} and C_{Du} determine the final voltage V_{Mu} and V_{Du} as well as the stored energy. Fig. 4.15(b) shows a zoomed portion of Fig. 4.15(a). As shown in Fig. 4.15(b), when M_u is turned on, V_{Mu} and V_{Du} drop to zero and there is a bump in the device current. The equivalent circuit of this instant is shown in Fig. 4.16(b). As shown in Figs. 4.15(b) and 4.16(b), when M_u is turned on, energy stored in C_{Mu} is lost and energy in C_{Du} is transferred into parasitic inductance, therefore driving a current bump. Part of this energy is lost in M_u while the rest is retrieved by the resonant capacitor. Device currents during these two sub-modes are determined as follows.

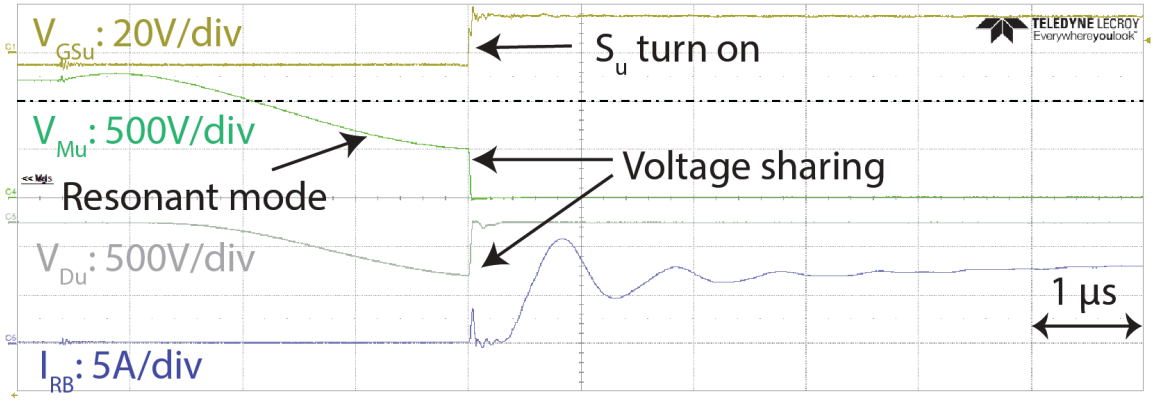
During the time where V_{Du} drops to zero:

$$I_{sw} = e^{-\alpha t} \frac{V_{cr0}}{L\omega_d} sin(\omega_d t), \tag{4.6a}$$

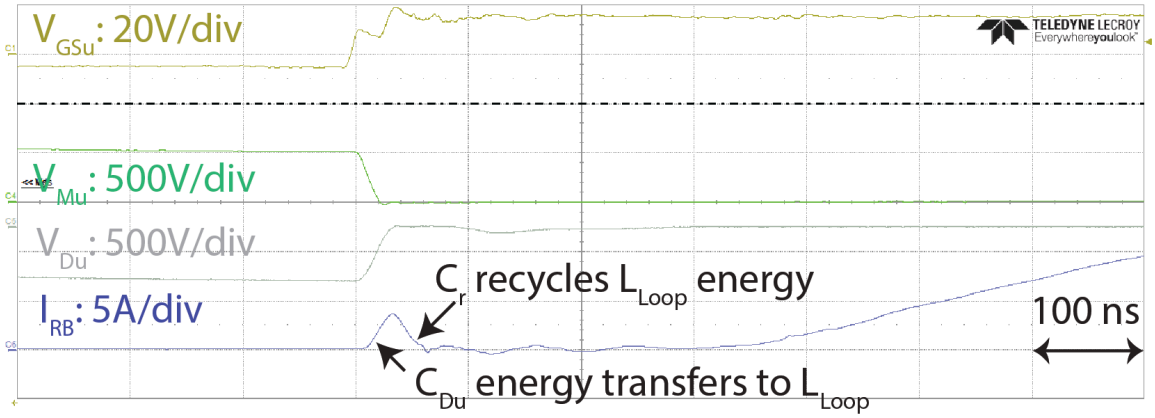
During the time where energy is recycled by C_r:

$$I_{sw} = \frac{V_{c0}}{L\omega_d} - \frac{V_{diff}}{L_{loop}} t, \tag{4.6b}$$

where $\alpha = \frac{R}{2L_{loop}}$, $\omega_d = \sqrt{\frac{1}{L_{loop}C_{D1}} - \frac{R^2}{4L_{loop}^2}}$, $V_{diff} = V_{Cr,pk} - V_{dc1}$, and R is the lumped wire resistance. Switching losses calculated by (4.1) only include the losses driven by C_{Du} rather than C_{Mu}. Because of lack of access to the device channel current, the part



(a)



(b)

Figure 4.15: Voltage sharing during turn-on transition using discrete 1.7 kV MOSFET/ Diode.

of switching losses caused by C_{Mu} is not measurable by (4.1). Therefore, calculation of capacitor stored energy before turning M_u on is an estimation for this loss, which is 5 μJ under the 1.2 kV, 8 A test condition.

Switching losses of the 1.7 kV device are calculated under different voltage and current levels, with consideration of the turn-on voltage sharing phenomenon, as shown in Fig. 4.17. Comparing the power losses calculated at 1.2 kV, 8 A for both soft- and hard-switching scenarios, the power losses under soft switching are reduced by 94.5%. Total switching losses under soft-switching condition are 13.9 μJ of which 10.8 μJ is originating from C_{Su} and C_{Du} voltage sharing. Soft switching helps to reduce majority portion of the switching losses while turn-on voltage sharing contributes to a major portion of the overall

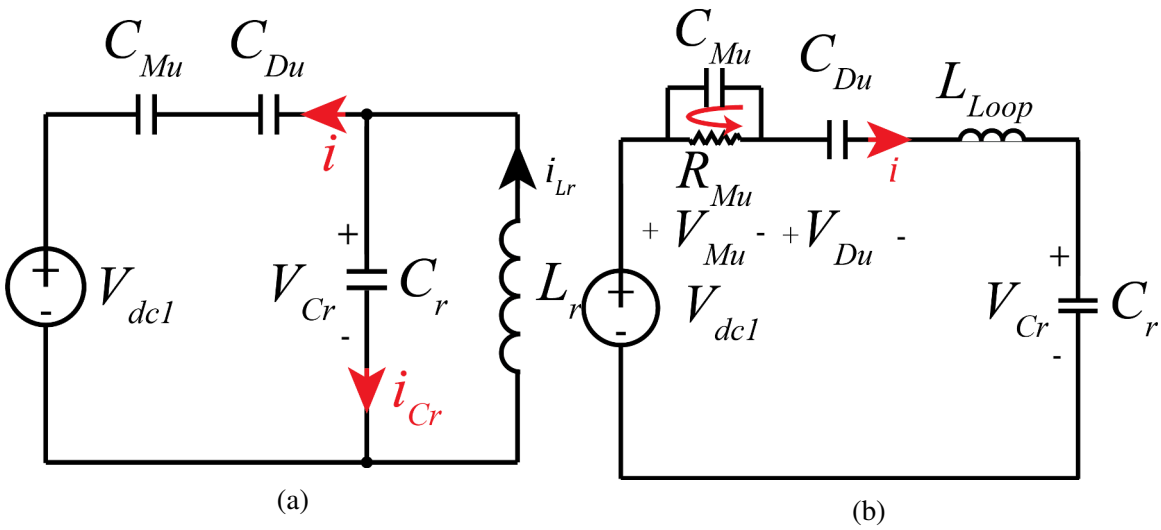


Figure 4.16: Equivalent circuit during (a) resonant mode and (b) S1 turn-on transition.

switching losses. In the 3.3 kV module, because of the lack of access to individual MOSFETs or diodes, turn-on losses cannot be calculated. However, using the same mechanism as described in (4.6) for the 1.7 kV module, the turn-on losses in the 3.3 kV module can be estimated as 75 μJ, which result in a 96% switching losses reduction at 1.6 kV, 25A.

4.10 Conclusions

There is a pressing need to build high-voltage power converters, such as solid-state transformers, for direct grid-connected applications. This has been driving the development and adoption of SiC power devices rated at 3.3 kV to 15 kV. However, SiC device operation in typical voltage source converters is accompanied by high dv/dt of 30-50 kV/μs, causing severe EMI problems in real converters. New topologies such as the S4T appear attractive because they realize zero-voltage switching giving low switching loss and low EMI but require RB devices operating under ZVS conditions in a current-source structure – data for which is simply not available from manufacturers or from literature. Most of the available device characterization data has been for devices with anti-parallel diodes, not with series-connected diodes.

This chapter presents the detailed test results and model extraction for 3.3 kV 45 A SiC

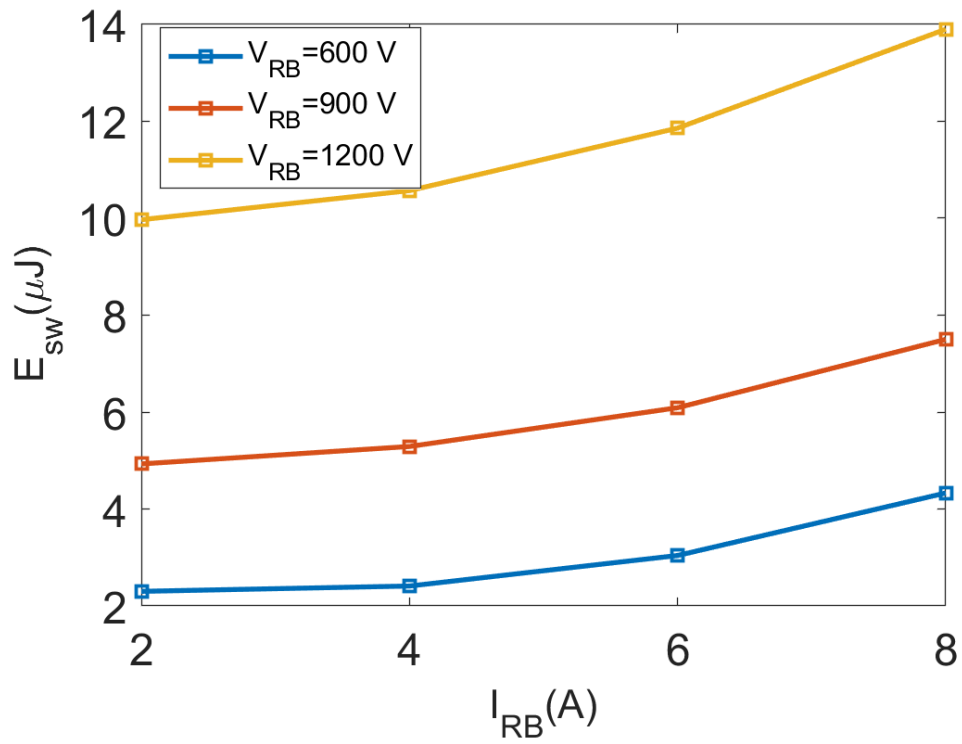


Figure 4.17: Power loss of 1.7 kV RB-device under soft-switching condition considering turn-on voltage sharing.

module with five RB devices in the package. A novel test-bed was designed and built for this characterization and model extraction of RB modules under both hard-switching and ZVS conditions. The testing helps to generate a parasitic and loss model for the RB devices, showing that switching losses are reduced by as much 96% , while dv/dt is reduced from 30 kV/μs to $<$ 1 kV/μs. The testing also helps to identify unexpected dynamic voltage sharing issues between the series diode and MOSFET. It was shown that this voltage sharing issue within an RB module (between the switch and the diode) results in a marginally higher switching loss.

CHAPTER 5
USE OF RB SIC MODULES IN CURRENT-SOURCE ZERO-VOLTAGE-SWITCHING CONVERTERS

In Chapter 4, it was shown that the dynamic voltage sharing between the diode and the switch within an RB module causes slightly increased switching losses even under soft switching conditions. The same phenomenon when extended to two RB modules results in a much larger problem, i.e., an increased voltage stress. In a traditional VSC, the free-wheeling diodes (FWDs) limit the maximum voltage across any devices to be equal to the DC bus voltage. In a CSC, such as the S4T, two RB modules together have to block V_{in} – V_{Cr}. Since V_{Cr} varies from $+V_{in}$ to $-V_{in}$, the two RB modules have to block a maximum of $2 \cdot V_{in}$. There is no FWD equivalent in CSCs to ensure $2 \cdot V_{in}$ voltage is shared equally between the two RB modules. This section explains the dynamic voltage sharing issue between two RB modules, using a DC-DC S4T converter as an example. In addition, a modified gating strategy for the RB modules in the S4T, which enables full realization of the benefits of soft switching, is presented.

5.1 Suppression of Gate Voltage Overshoot

As shown in Fig. 4.15(a), when the 1.7 kV module is characterized, the gate-source voltage has an additional 5 V stress during turn-on. This is due to the common source inductor (CSL) between the gate loop and the power loop, as shown in Fig. 5.1. The resonance between the device capacitance and L_{loop} is coupled to the gate loop by the CSL. This issue can be solved by either using a Kelvin source like in the 3.3 kV module or increasing the gate resistance or capacitance to suppress the resonance coupled to the gate loop. The following discussion will be focused on the latter method.

Under hard-switching condition, increasing the gate resistance or capacitance is not

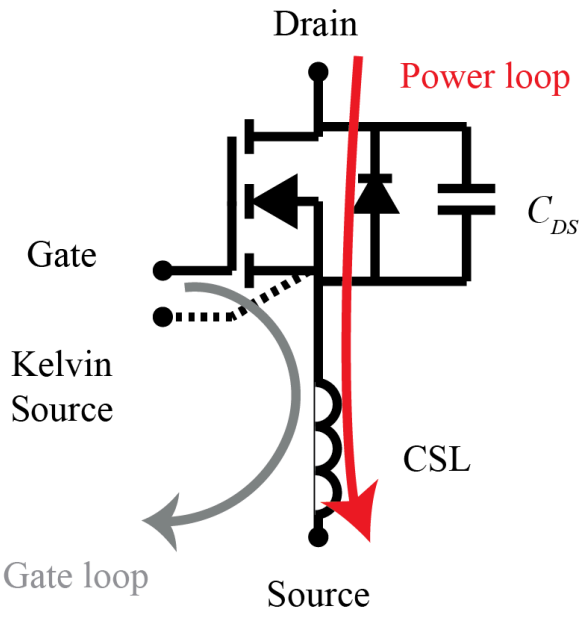


Figure 5.1: Power and gate loops coupled by the CSL in absence of a Kelvin source.

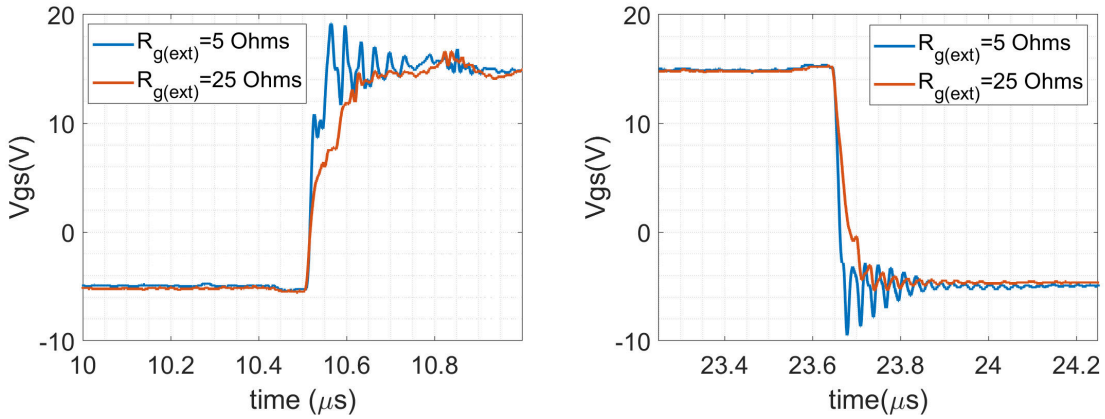


Figure 5.2: Switching waveforms with different $R_{g(ext)}$ (a) turn-on and (b) turn-off transient.

acceptable as it increases the switching losses and the risk of crosstalk. However, when using soft switching, the switching losses are no longer of a concern and the value of dv/dt is much lower compared to hard-switching condition [93]. Therefore, the risk of crosstalk by using a higher gate resistance or capacitance is eliminated. As shown in Fig. 5.2, when the applied gate voltages are -5 V and 15V, with a 5 Ω external gate resistance ($R_{g(ext)}$), the

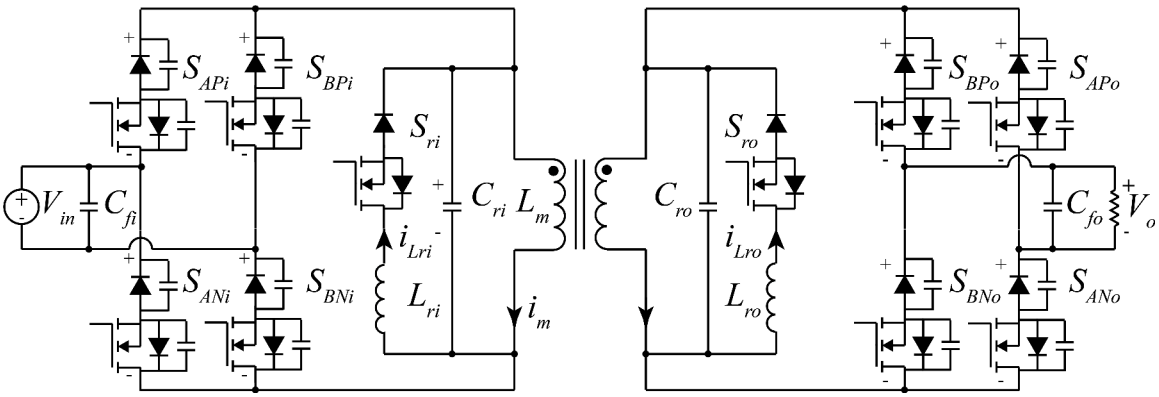


Figure 5.3: Circuit diagram of the S4T with parasitic capacitances.

gate-source voltage stresses are -8.6 V and 20 V, respectively, while with a 25 Ω external gate resistance ($R_{g(ext)}$), they become -5.4 V and 17 V, respectively. Both positive and negative voltage stresses are suppressed by increasing the gate resistance.

5.2 Turn-on and Turn-off of Main Devices

5.2.1 Turn-on and Turn-off of Main Devices without Considering the Voltage Sharing within an RB Device

Conventionally, switching devices of the S4T that are expected to carry the current, are turned on and off at the beginning and end of that particular conduction mode, respectively [20]. However, this gating strategy can result in an additional voltage stress across the devices because of the dynamic voltage sharing issues discussed in the previous section. Fig. 5.3 shows the circuit diagram of the S4T for DC-DC applications where device parasitic capacitances and voltage polarities are represented. Fig. 5.4 shows the devices carrying current in each mode and Fig. 5.5(a) shows the voltage of each RB-device using the conventional gating strategy. At t_2, the S4T is in the charging mode with S_{APi} and S_{BNi} being on, as shown in 5.4(b). The charging mode ends at t_3 with turning S_{ANi} on and turning S_{BNi} off while the state of S_{APi} remains the same, as shown in 5.4(c). The two devices on the lower side of the input bridge are discharged in ZVS mode and S_{BNi} blocks the input

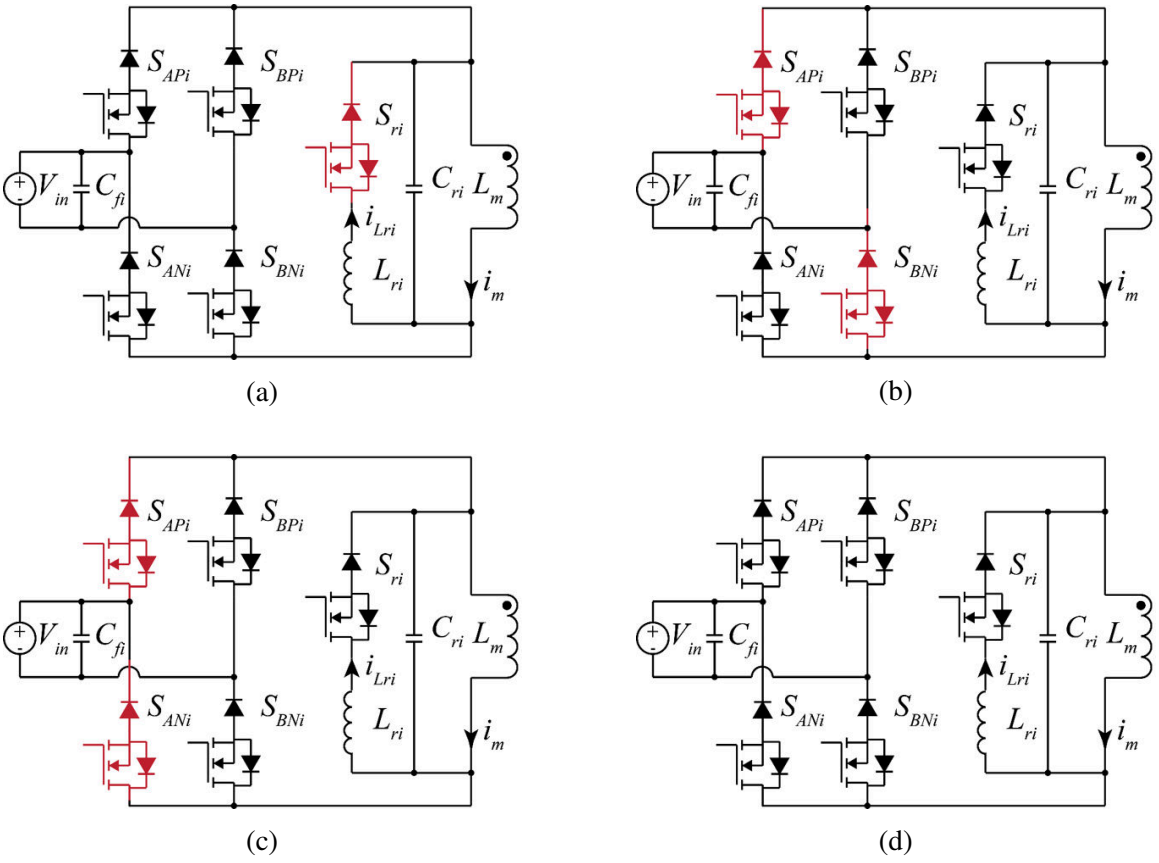
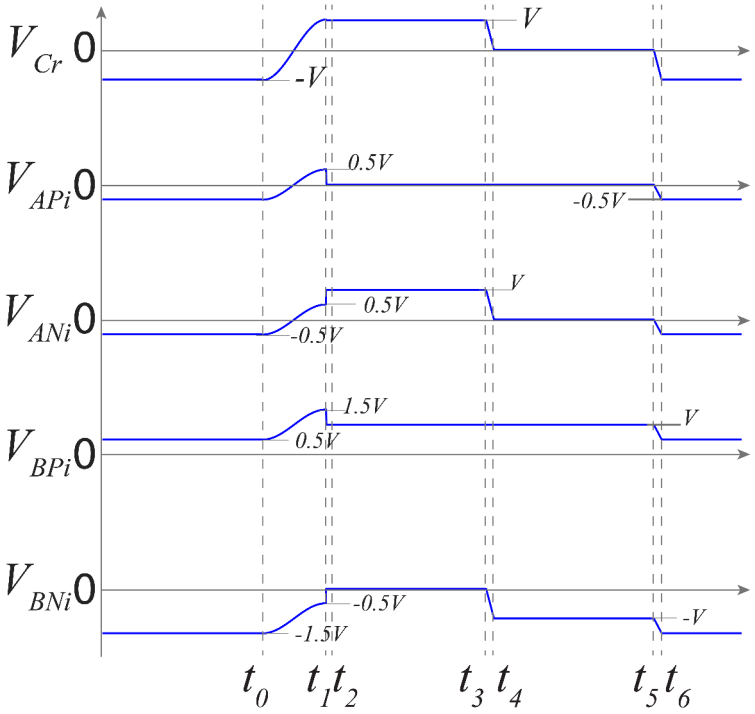
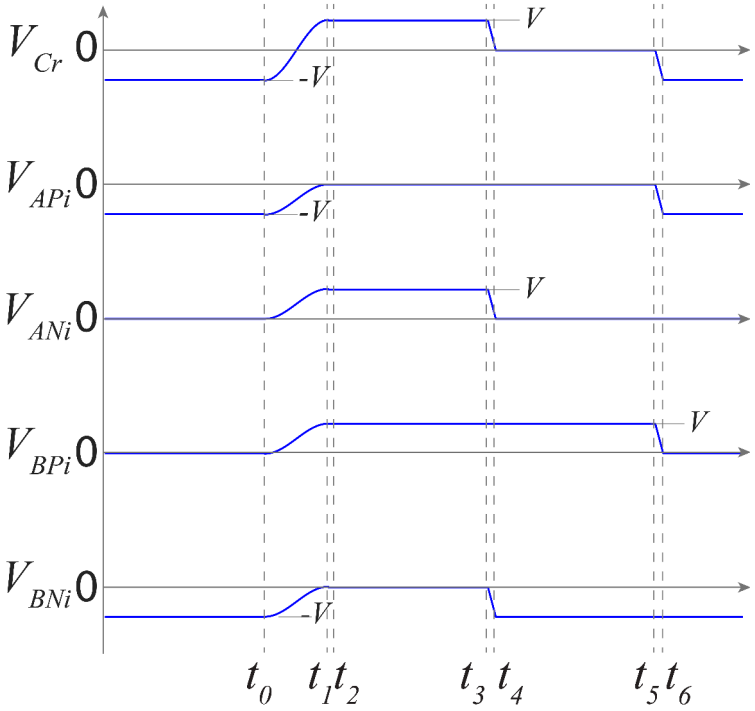


Figure 5.4: Turned-on RB-devices of the input bridge of S4T in different mode using conventional gating strategy (a) resonant mode, (b) charging mode, (c) freewheeling mode and (d) discharging mode.

voltage at t_4. After t_5, the freewheeling mode is over, and the input bridge is inactive with all its devices turned off, , as shown in 5.4(d). Therefore, all devices of the input bridge are discharged in ZVS mode and ΔV of each RB-device during the ZVS mode from t_5 to t_6 is half of the ΔV_{Cr}. When the input and output voltages are the same, S_{BNi} is blocking 1.5 p.u. voltage at t_6 compared to the nominal operating voltage as shown in Fig. 5.5(a). At t_1, when the resonant mode is over and prior to turning S_{APi} and S_{BNi} on, V_{APi} and V_{BNi} are not zero and their turn-on losses are not negligible. Therefore, the benefits of the S4T in terms of controlled dv/dt and absence of switching losses are dismissed when relying on the conventional gating strategy. The root cause of this phenomenon is the unequal voltage sharing of the upper- and lower-side RB-devices even though the total voltage is



(a)



(b)

Figure 5.5: Voltage of each RB-device of the input bridge of the S4T using (a) the conventional gating strategy and (b) the proposed turn-on scheme.

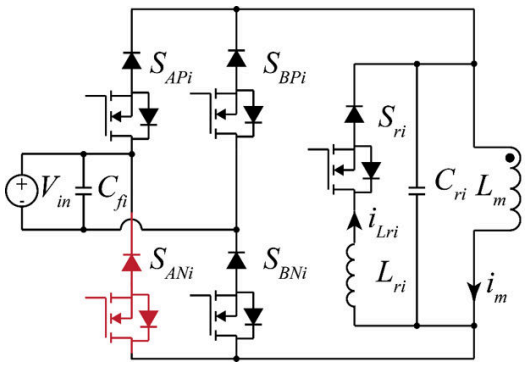
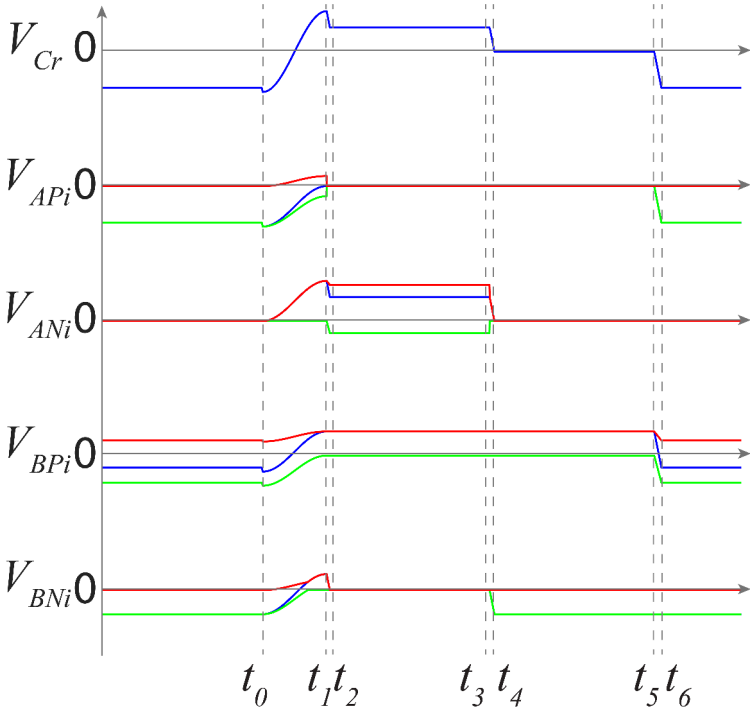


Figure 5.6: Turned-on RB-devices of the input bridge of S4T in discharging mode using proposed gating strategy.

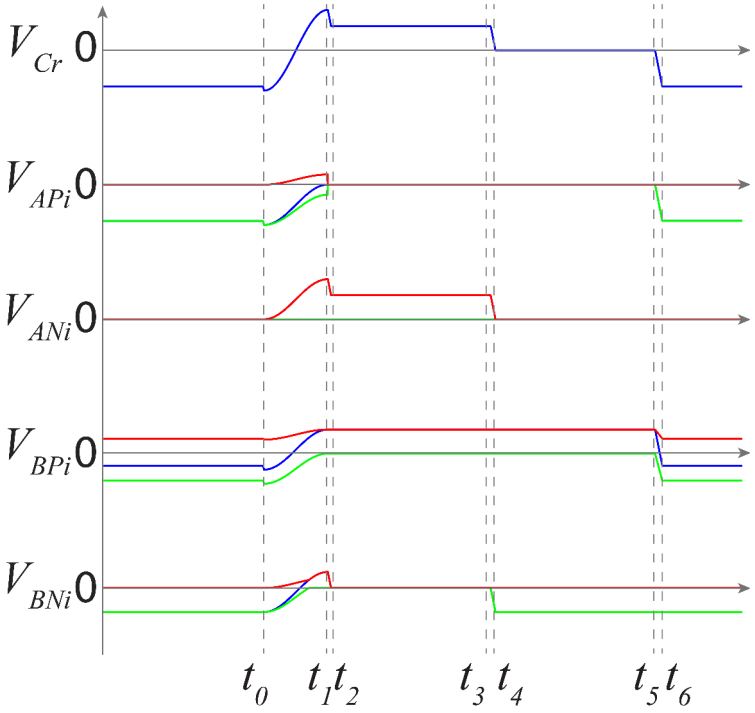
controlled by C_r. A proper gating sequence is required to control the voltage sharing of each RB-device. When the input bridge is inactive, instead of turning both S_{APi} and S_{Ani} off as shown in Fig. 5.4(d), only S_{APi} is turned off as shown in Fig. 5.6. By keeping S_{ANi} on, only the upper-side RB-devices of the input bridge are discharged in ZVS mode from t_5 to t_6. Consequently, the additional voltage stress is eliminated and V_{APi} and V_{BNi} become zero prior to turning on at t_1. The same strategy can be applied to the output bridge. When the output bridge is inactive, S_{ANo} is turned on to control the voltage sharing of each device.

5.2.2 Turn-on and Turn-off of Main Devices Considering the Voltage Sharing within an RB Device

Besides the unequal voltage sharing phenomenon of the upper- and lower-side RB-devices, voltage sharing between the MOSFET and diode within the same RB-device in the S4T needs to be addressed as well. As shown in Fig. 5.7(a), uneven voltage sharing between the MOSFET and diode of S_{APi} occurs after resonant mode. This is the same phenomenon as discussed in Chapter 4. This uneven voltage sharing cannot be avoided by the gating strategy. However, during the ZVS mode from t_1 to t_2, uneven voltage sharing between the MOSFET and diode of S_{ANi} occurs. The MOSFET is discharged to a negative voltage which consequently contributes to turn-on losses. Instead of turning S_{ANi} on in



(a)



(b)

Figure 5.7: Voltage of each RB-device (blue), MOSFET (green) and diode (red) of the input bridge of S4T using the proposed gating strategy (a) without pre-turn-on and (b) with pre-turn-on.

its corresponding vector, S_{ANi} can be turned on after the resonant mode. As shown in Fig. 5.7(b), by applying this strategy, the voltage is only blocked by D_{ANi} and the turn-on losses of S_{ANi} is eliminated. The same strategy can be extended to the output bridge. As discussed, this pre-turn-on strategy saves only a small portion of the switching losses but adds to control complexity and safety concerns, which are not preferable. Unless there is a very undesired unequal voltage sharing between the MOSFET and diode, the improvement by the pre-turn-on strategy is not significant.

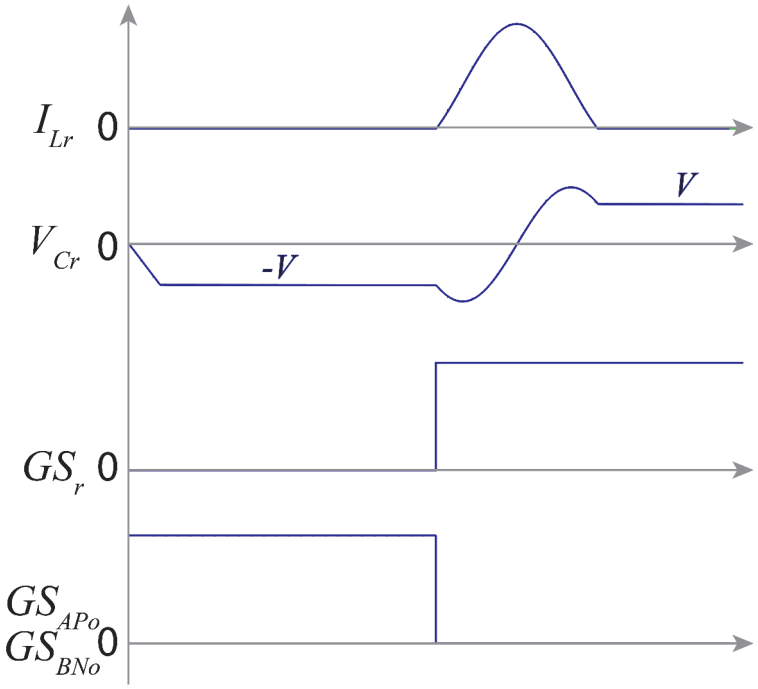
5.3 Turn-on and Turn-off of Resonant Devices

5.3.1 Turn-on of Resonant Devices

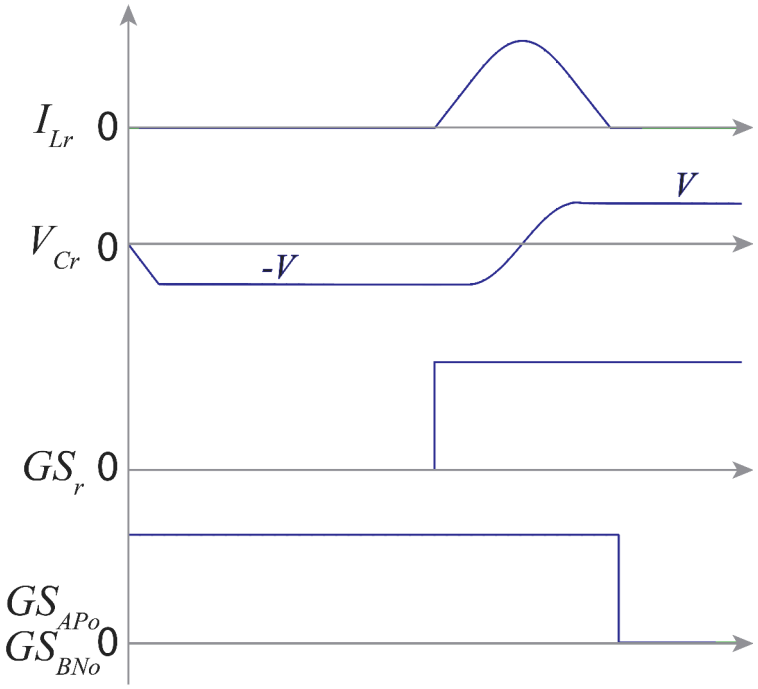
In the previous section, it is discussed that an undamped resonance can occur if S_r is not turned off with zero current. For practical implementation, to ensure ZCS turn-off of S_r, the gate-source signal of S_r (GS_r) can stay high until mode 1 ends. The current in S_r will decrease to zero and S_r is reversely blocked during the charging mode.

5.3.2 Turn-off of Resonant Devices

As shown in Fig. 5.8(a), when S_r is turned on, a resonant voltage stress is added to the nominal blocking voltage. To ensure ZVS, after resonant mode, it is necessary for V_{Cr} to be higher than the voltage in mode 1. Therefore, one more ZVS mode to discharge V_{Cr} may be required before entering the resonant mode. Consequently, the maximum voltage blocked by each device is higher than the voltage at which the converter is operating. Generally, this overvoltage can be reduced by sizing the resonant components correctly. However, if the S4T is operating under boost condition, this overvoltage can be eliminated by properly turning S_r on and S_2 off. Under boost condition, GS_{APo} and GS_{BNo} turn low at the time when GS_r turns high. Therefore, i_L continues to discharge C_r until i_{Lr} reaches i_L and maximum V_{Cr} is higher than the operating voltage. Since the negative V_{Cr} is always higher than the voltage in mode 1, additional ZVS mode can be skipped. GS_r can turn high before GS_{APo}



(a)



(b)

Figure 5.8: Voltage of each RB-device of the input bridge of S4T using (a) the conventional gating strategy and (b) the proposed turn-on scheme.

Table 5.1: Switching consideration for the main and resonant devices in S4T

	Main devices	Resonant devices	
	turn on off	turn on	turn off
Concern	Voltage Sharing	Over voltage	Undamped resonance
Impact	Voltage stress Losses EMI	Voltage stress	Current stress Loss
Strategy	Keep one RB device on when this bridge is inactive	Turn on before main devices off	Turn off after 1st charging mode
Condition		Boost operation	

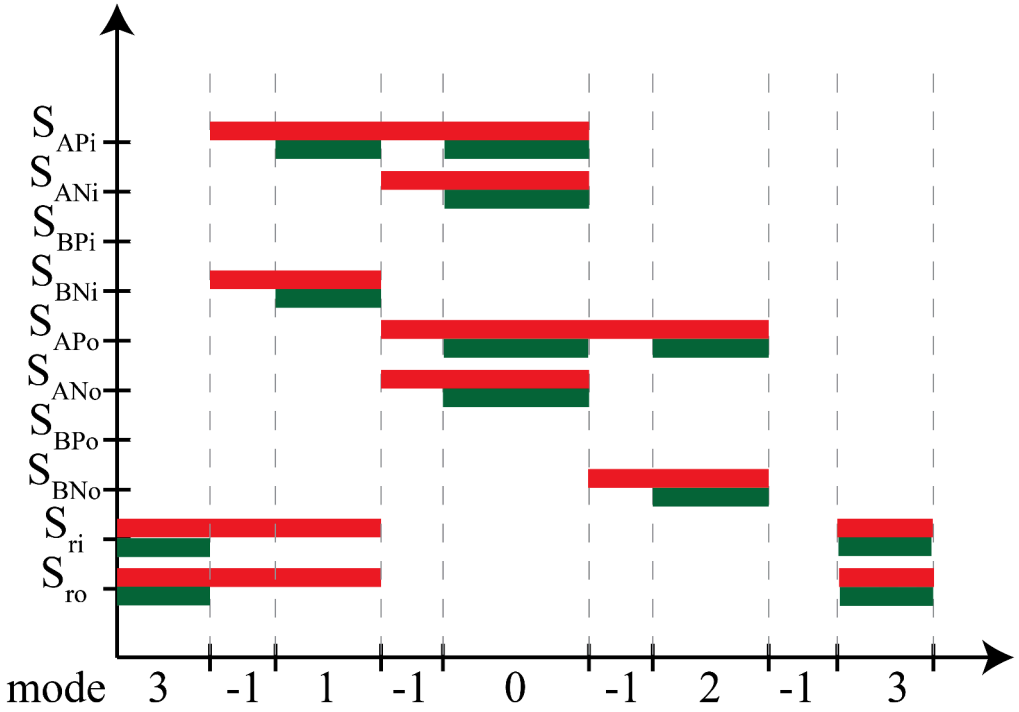
and GS_{BNo} turn low and i_L will not discharge C_r, thereby maximum V_{Cr} equals the operating voltage.

5.4 Switching Sequence of the S4T

Based on the previous discussion, the switching sequence of the conventional voltage/flyback type current-source converters, such as the one presented in [48, 94, 95] cannot be applied to the S4T. To fully utilize the benefit of the S4T, a new switching sequence is proposed. Table 5.1 summaries the key considerations for the turn-on and turn-off states of the main and resonant devices. Fig. 5.9 shows the gate signals applied to each RB-device of the S4T in which a red bar shows when the gate-source voltage of a specific device is high while a green bar shows when the DC link current is flowing through a specific device. The nomination of modes is similar to that shown in Fig. 4.3, in which mode 1 is the the charging mode, mode 2 is the discharging mode, mode 3 is resonant mode, mode -1 is ZVS mode and mode 0 is freewheeling mode.

5.5 Converter Verification

The proposed switching sequence is applied to a S4T prototype shown in Fig. 5.10. Fig. 5.11 shows the voltage sharing impact on the device voltage during turn on transition and verifies the effectiveness of the proposed switching sequence. Fig. 5.11(a) shows the



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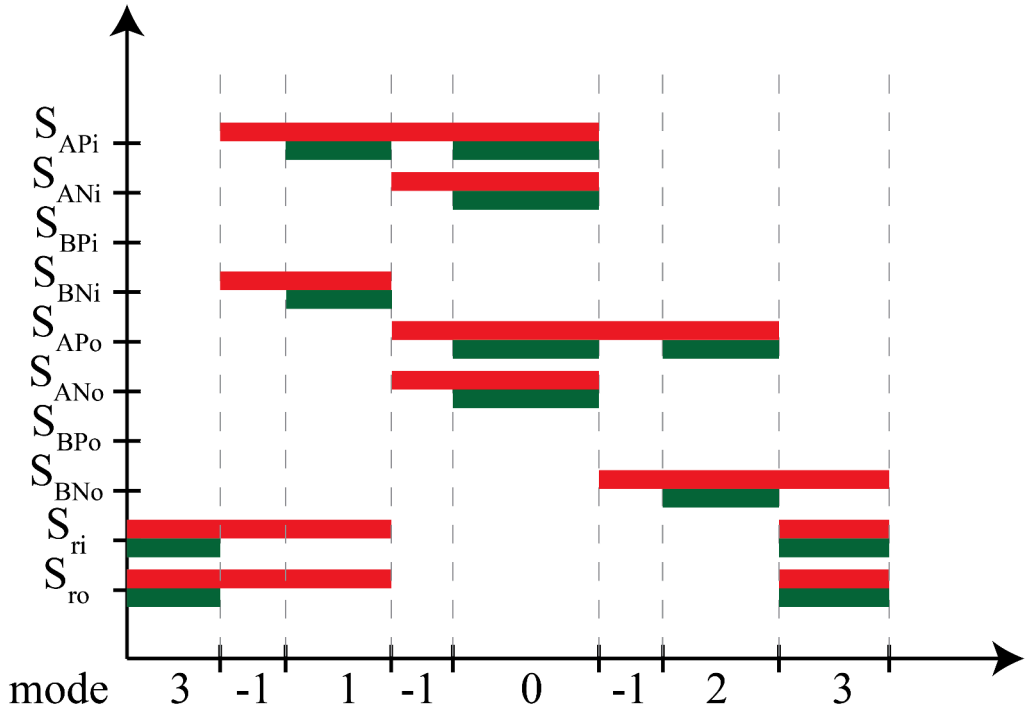


(b)

Figure 5.9: The proposed switching sequence of the S4T for (a) general cases and (b) boost operation.

waveforms of the S4T using the conventional switching sequence. As shown, the RB-device is turned on with hard-switching and the dv/dt is high. Fig. 5.11(b) shows the waveforms of the S4T using the proposed switching sequence. The RB-device is fully ZVS and dv/dt is controlled. Fig. 5.11 also confirms suppression of the additional voltage stress on C_r and the effectiveness of the proposed switching sequence under boost operation.

5.6 Conclusions

In previous chapter, it was shown that a voltage sharing issue within an RB module (between the switch and the diode) exists. In this chapter, it was shown that the same phenomenon of dynamic voltage sharing, when extended to two RB modules (one upper RB module and one lower RB module) in the S4T, causes additional voltage stress (up to 1.5 pu) across each RB module. Modified switching schemes to limit this voltage stress when the RB modules are used in such converters are presented and verified through an

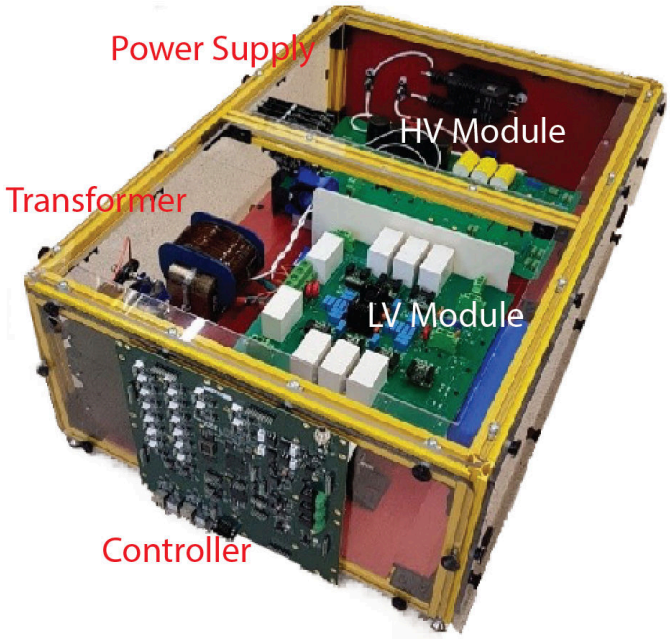
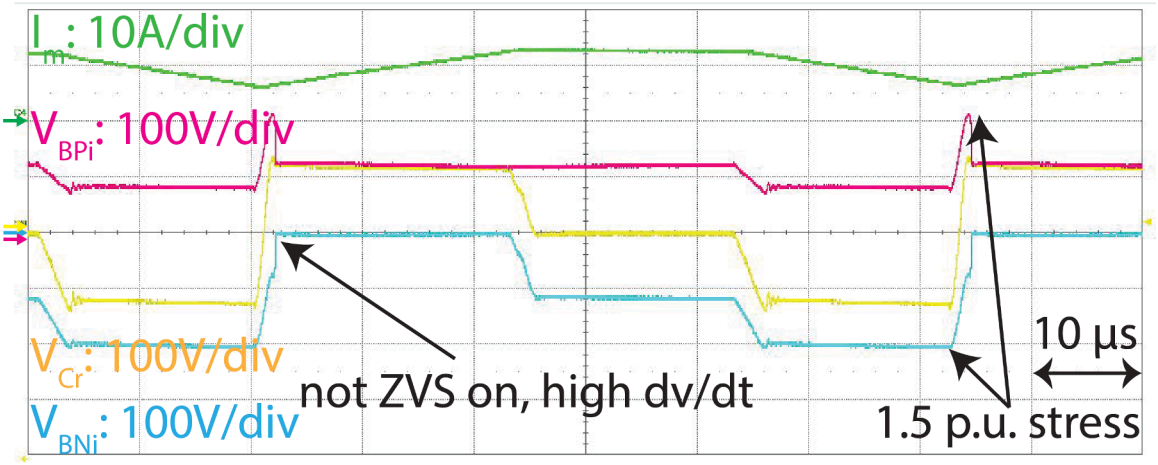
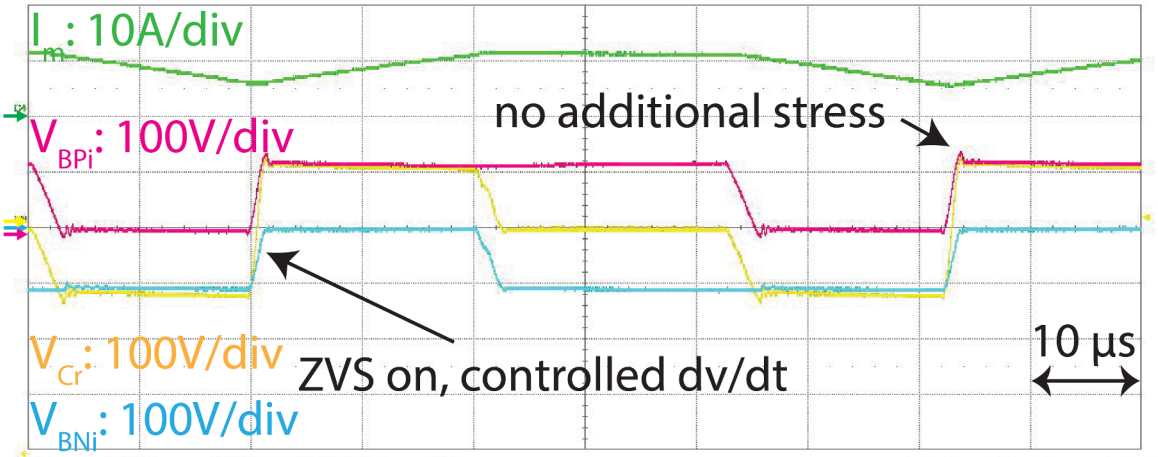


Figure 5.10: Image of the 25 kVA 2.5 KV DC/ 600 V DC S4T module.



(a)



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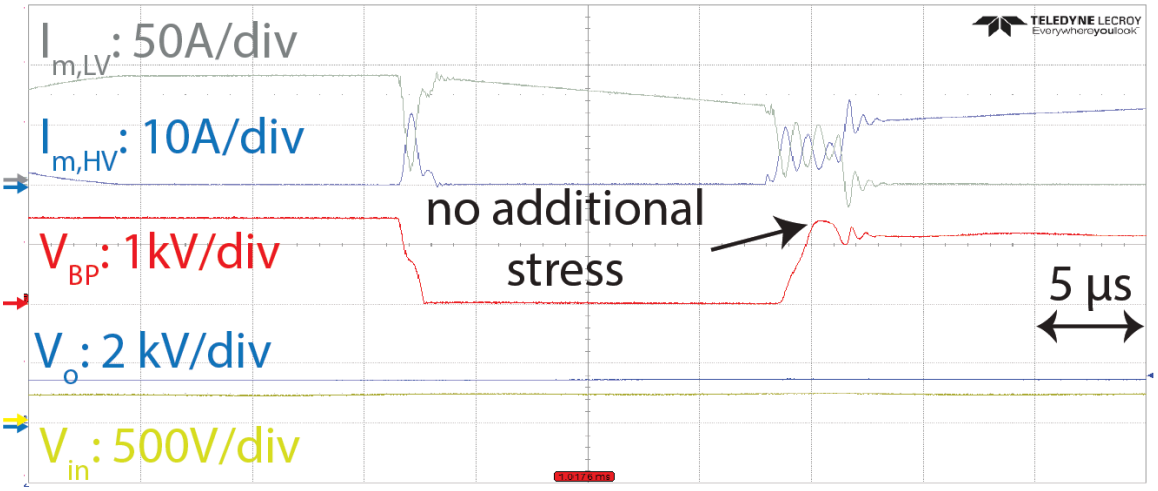


(c)

Figure 5.11: Waveforms of total RB-device voltage in the S4T using (a) the traditional switching sequence at 100V; and (b) the proposed switching sequence at 100V (c) the proposed switching sequence at 1.5 kV, 10 kVA.

S4T prototype rated at 1.5 kV, 10 kVA. In addition, a proper switching scheme for resonant switches are also discussed to reduce the voltage stresses.

CHAPTER 6

REAL-TIME MODELING AND HIL SIMULATION OF STACKED LOW-INERTIA CONVERTERS WITH SOFT-SWITCHING AND FAST DYNAMIC CONTROL

In this chapter, a DC-DC M-S4T is chosen as an example of a low-inertia converter, as shown in Fig. 6.1. Although DC-DC M-S4T is a specific example, the discussion and methodologies in this chapter can be generalized to any other modular low-inertia converter. Because of the fast-dynamic nature in low-inertia converters, all non-linearities and delays become significant in implementing deadbeat-like control algorithms. RT modelling and simulation with CHIL helps to investigate and verify such fast control algorithms. The simulation platforms like Opal-RT help to increase the simulation speed compared to the MATLAB/Simulink simulation in a single-core desktop computer. In the traditional VSCs, HIL simulation can operate in real time with no time step limitations because of the existence of high-inertia components like large inductors and capacitance in the circuits. However, for the S4T, because of its low-inertia nature and the existence of the resonant mode during its operation, the time step limits performance of the simulation of the S4T. A simulation model with high fidelity and reasonable time step is required for simulating such converters. This enables to perform HIL simulation to verify and improve performance and accuracy of control algorithms considering all non-linearities associated with the sensing and controller delays. In this chapter, a quasi-real-time (QRT) HIL model is proposed to address the challenges associated with RT modeling of such low-inertia converters and converters operating with resonant mode and the benefits derived from HIL simulation in terms of verification of the MPPS control and improving the controller performance are discussed.

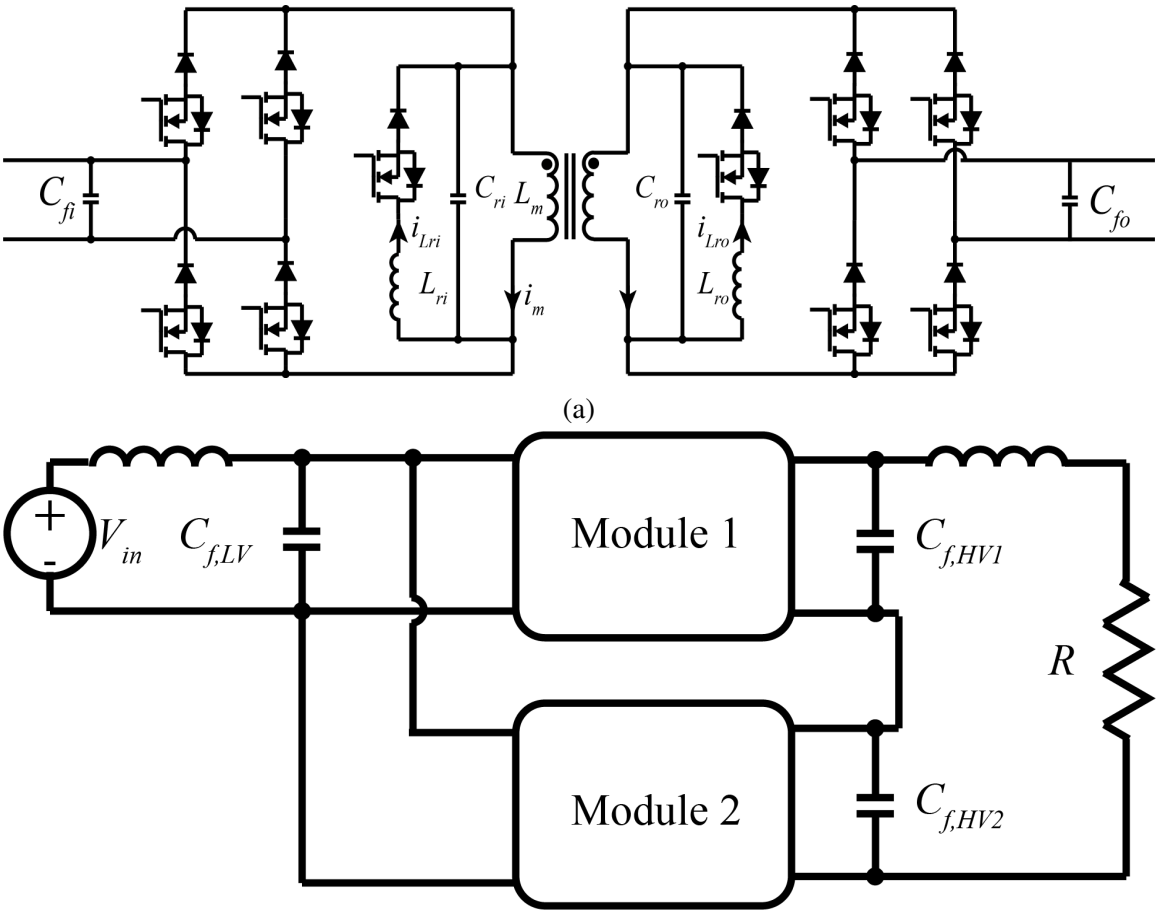
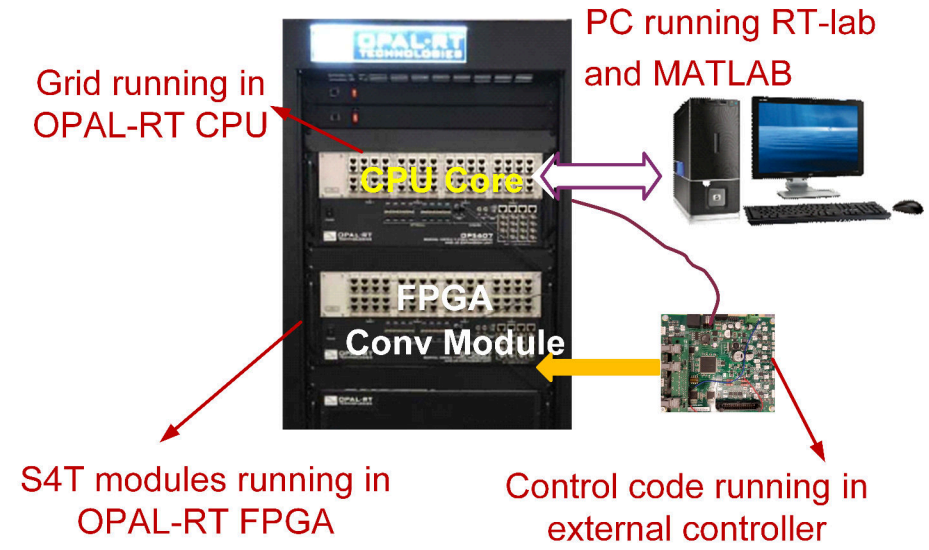


Figure 6.1: (a) the DC-DC S4T circuit topology and (b) a two-module stacked M-S4T.

6.1 HIL Simulation of S4T

The HIL simulation of the S4T is referred to the CHIL. Fig. 6.2(a) shows the connection of HIL simulation of S4T. The HIL platform used here is based on OPAL-RT system. In this configuration, the grid part of the converter which runs at a slow speed can be simulated in the CPU of the OPAL-RT system. The converter parts, i.e., the S4T modules which run at a much higher speed are required to be simulated in the FPGA of the OPAL-RT system. There are communication links between the CPU and FPGA of OPAL-RT internally so that the calculated data in both parts can be shared and merged. By using the I/Os on the OPAL-RT, the command and calculation of the simulated converter can be logged by an additional PC which is running the RT-lab, a specific software designed for OPAL-RT



(a)

(b)

Figure 6.2: (a) HIL simulation configuration and (b) I/Os of each OPAL-RT module.

system. Besides, external controller cards are used to connect to the simulated converter to send or receive signals and perform control algorithm. Fig. 6.2(b) shows the I/Os on the OPAL-RT unit.

6.2 Challenges in S4T Simulation and Implementation of MPPS

Although using HIL simulation as a tool to achieve rapid prototyping and simplifying the design process of power electronics VSCs is well-known , the use of HIL simulation on low-inertia converters such as the S4T needs further investigation. Several aspects including time step and converter size limitations and considerations of non-idealities need to be

addressed.

6.2.1 Time Step Limitations

As described earlier, resonant mode and state transition modes in the S4T operation are essential to ensure ZVS operation. However, because of the existence of these additional modes, simulation of the S4T requires much slower time step than that of other converters switching at a similar frequency. Typically, the switching frequency of the S4T is in the range of 16-20 kHz. To simulate the S4T switching at these switching frequencies, time step as low as 0.1 μs is required to capture the dynamics and interaction in these two modes since the time span of the two modes is around 1 - 3 μs while for the traditional VSCs, the time step could be larger than 10 μs. The difference in the time step significantly slows down the simulation speed for the S4T, i.e., simulating 1 second in real-time takes 3800 seconds with a single-core simulator on a desktop PC. As more switches and passive elements are used in the simulation of stacked converters, i.e., M-S4T for railway applications, this can become very restrictive. Simulating 1 second in real-time of the S4T can take 8 hours.

An RT platform, such as OPAL-RT, simulates based on a multi-core structure and can effectively accelerate the simulation speed compared to the conventional PC-based simulation. In addition, RT platforms can integrate the controller verification in the simulating process, called HIL. The structure of the S4T simulation using OPAL-RT is shown in Fig. 6.3. The entire simulation structure consists of an OPAL-RT unit, a controller and an oscilloscope. The OPAL-RT unit is mainly comprised of one or multiple FPGA-based electric hardware solvers (eHSes) and several analog /digital inputs /outputs (AI /AO /DI /DOs). In the OPAL-RT unit, after acquiring the control input from the external controller through DIs, the eHS calculates the S4T circuit model and CPU samples the results for sensor output and data visualization through AOs. The external controller receives these sampled results like voltages and currents and generates the control command for the next cycle.

Table 6.1: Time step requirements in the S4T simulation

	Required time step by HIL (maximum)	Achievable time step by OPAL RT (minimum)
Circuit simulation	0.1 μs	0.5 μs
Sensor delay	0.1 μs	20 μs
ADC sampling	3 μs	20 μs
Waveform visualization	0.1 μs	20 μs

In OPAL-RT, the eHS calculation time step impacts the calculation accuracy in the same way as the single-core PC-based simulation. In addition, the CPU sampling time impacts the data sampling speed which can be used to configure the sensor bandwidths and delays. Because the CPU is a relatively slow component compared to the FPGA-based eHS, CPU sampling time is much larger than calculation time step. For the simulation of a single module S4T, i.e., the smallest possible calculation time step is 0.5 μs, which is larger than the required minimum time step of 0.1 μs and the corresponding CPU sampling time is 20 μs. A summary of the maximum required time step by HIL simulation and the minimum achievable time step by OPAL-RT is shown in Table. 6.1.

To ensure an accurate result with high resolution, the RT model needs to be scaled down as a quasi-real-time (QRT) HIL model. Considering the implementation complexity in the digital controller, the scaling factor should be power of 2 (2^X). The factor of 256 is chosen to be appropriate for the modeling of the S4T, which means that the values of all the reactive components like inductors and capacitors are 256 times larger while the resistances and voltage/current sources remain unchanged in the model and the switching frequency in the controller is decreased by a factor of 256. Besides the QRT HIL model, the time used in FPGA is also scaled by the same factor. Since the interrupt of DSP is provided by the FPGA, the DSP is scaled down naturally and its code remains unchanged. Table 6.2 lists the modifications in simulation model and FPGA/DSP code to simulate this scaled-down system. With these modifications, the QRT HIL model can perform simulation of 1 second real-time operation in 256 seconds compared to 3800 seconds using the single-core simulator. For systems with more components, the speed of simulation of the QRT HIL

Table 6.2: Modifications in the QRT HIL model

	Reactive component value	Time	Bandwidth
QRT HIL converter model	$\times$256	$\times$256	$\div$256
FPGA code	$\times$256	$\times$256	$\div$256
DSP code	No change	No change	No change

model can be 100 times faster compared to the single core simulator.

6.2.2 Modeling of Non-idealities of the Controllers

As discussed in Chapter 2, to control the stacked low-inertia converters, a novel MPPS control is used [28]. The MPPS control achieves multiple objectives including sharing series-connected side voltage equivalently and maintaining DC link current with high-bandwidth control. However, implementation of the MPPS is challenging as it is a cycle by cycle control using accurate circuit model to calculate the duty cycle for the next operating switching cycle. Therefore, all the non-idealities in a controller including ADC delays, controller bandwidth, communication delays, scaling errors, etc. impact controller performance. The delays and limitations in the bandwidth of the sensors, ADCs, and communications need to be understood. As shown in Fig. 6.4, for the delays and bandwidth of the sensors in the simulation model, a first-order digital low-pass filter (LPF) based on the CPU sampling time is added to each AO using the bandwidth used in real sensors. In the LPF, $a = T_{CPU}/(T_{CPU} + 1/BW)$. It should be noted that the bandwidth of the LPF is selected as 1/256 of the real value since it relates to the operation time. The sensor delays are added by the term z^{-n} , where *n* is the multiple of the CPU sampling time. By using the QRT HIL model, the impact of the non-idealities in the controller such as ADC bandwidth and delay, communication delay, etc. can be tested and verified.

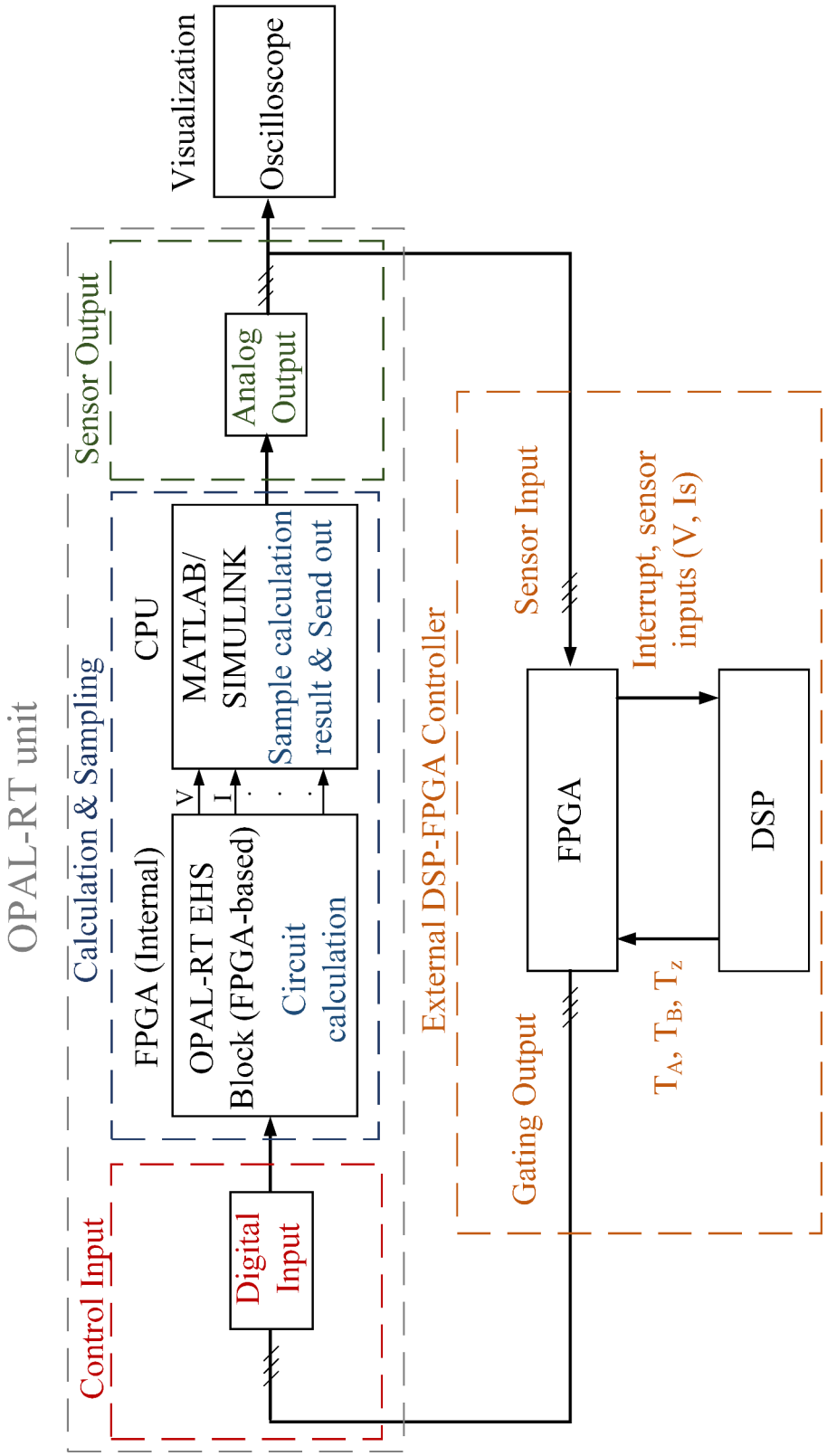


Figure 6.3: Block diagram of the S4T simulation in OPAL-RT.

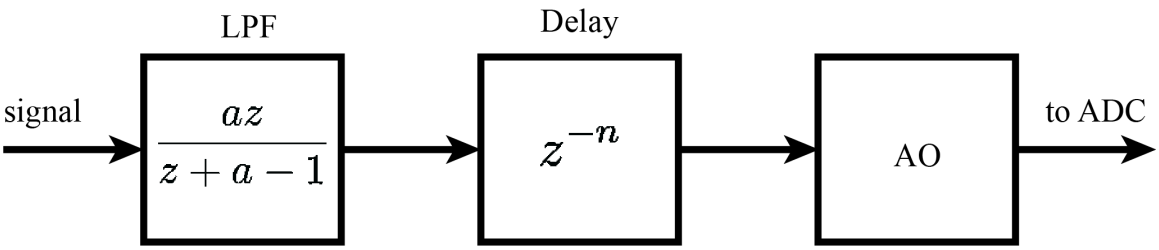


Figure 6.4: Model of sensor bandwidth and delay.

6.2.3 Converter Size Limitations

An OPAL-RT unit that uses eHS to solve electrical circuits has a limitation of the number of switches to be simulated in one simulation model. It is shown that the maximum number of switches and diodes can be solved by eHS x128 is 144, which means only 72 RB devices can be simulated in one OPAL-RT unit. Considering the S4T shown in Fig. 6.1(a) which utilizes 22 switches (10 switch/diode pairs and 2 leakage management diodes), each OPAL-RT unit is capable of simulating 6 S4T modules in one simulating project. Besides the limitation of the eHS x128 solving capability, the simulating time step becomes larger when simulating a system with 6 modules. Therefore, it can increase the scaled down factor, by which the total simulation speed is affected. The converter size is not only limited by the number of switches but the I/Os as well. The OPAL-RT unit used in this research has 16 analog outputs and 32 digital inputs, meaning that it can control 32 switches/diode pairs, which are 3 S4T modules in one simulation model. In addition, as discussed in the previous section, AOs serve as sensor outputs and visualization functions. Simulating 3 S4T modules requires 15 sensor outputs. In this sense, only one spare AO can be used to visualize key waveforms of each module including resonant capacitor voltage and resonant inductor current. Based on the above discussions, using only one OPAL-RT unit to simulate the M-S4T with more than 3 modules is impractical. Therefore, utilizing multiple OPAL-RT units to simulate a converter with higher number of modules is required.

To distribute the simulation tasks into multiple modules, a method to decouple S4T in several parts is required. Because of the modular nature of the M-S4T, only the interaction

between modules need to be solved. Fig. 6.1 shows the overall circuit used in the simulation while Fig. 6.5 shows the decoupled circuits. Each part of the decoupled circuit is simulated in one OPAL RT unit. Among all the decoupled parts, one part serves as the grid/load inter-connection, as shown in Fig. 6.5(a). This part uses the terminal current calculated by each S4T module and solves the terminal voltage of each module correspondingly. The terminal voltages are sent back to each corresponding S4T module for its own calculation of both side I_m, resonant capacitor voltage, etc. The same idea can be generalized to simulate 2 or 3 modules of the S4T in one OPAL-RT unit if a large converter, i.e., three-phase M-S4T, needs to be simulated. Since the size of each part is almost the same as a single model S4T, there is no issue with the number of devices simulated and AO/DI. Besides, the time step of the whole converter can be the same as a single-module S4T.

6.3 Comparison between HIL Simulation and Experimental Results

6.3.1 OPAL-RT Simulation Platform and Experimental Hardware

The accuracy of the QRT HIL model of the S4T is verified by comparing the simulation results of the QRT HIL model with the experimental results. The OPAL-RT system with 1 OP5700 unit and 5 OP5607 units is shown in Fig. 6.6. This system is comprised of 1 CPU and 6 eHSes and is used for the HIL simulation. As discussed previously, one S4T module is simulated in one OPAL RT unit and one of the units is used to simulate the grid inter-connection. For comparison, a 50 kW 5 kV DC to 600 VDC test setup has been built, as shown in Fig. 6.7. The circuit diagram is shown in Fig. 6.1. It consists of a 600 V DC source feeding the MVDC converter, which in turn is connected to a resistive load. In both HIL simulation and experimental test, an external DSP-FPGA based controller board is used, which means that the latencies and calculation errors are considered in the HIL simulation. The sensed variables in both cases are exactly the same and the sensor bandwidths are set as discussed previously. The code in the FPGA and DSP are the same except the differences mentioned in Table 6.2. As discussed previously, a scaling down

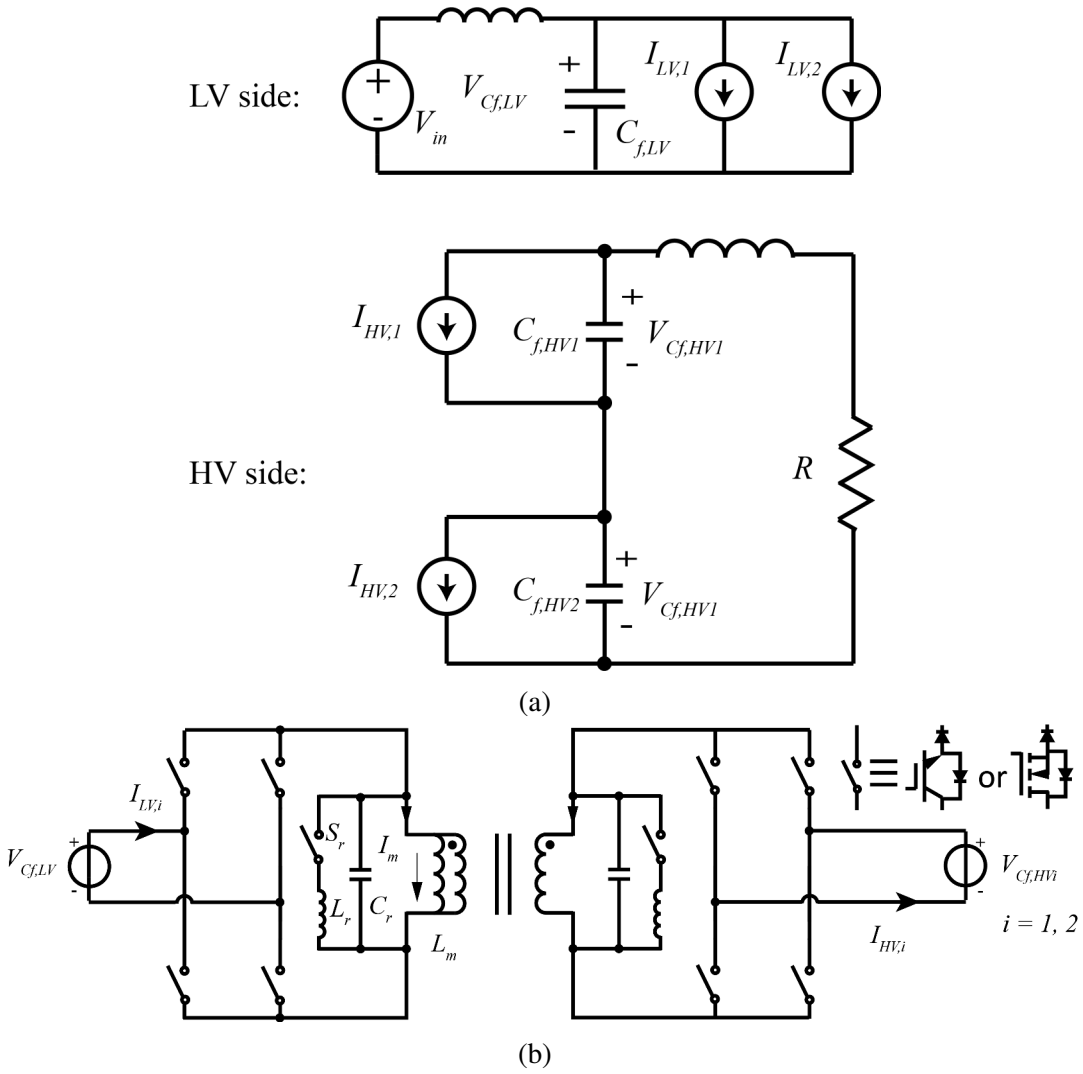


Figure 6.5: Decoupled M-S4T circuit for HIL simulation: (a) grid inter-connection sub-circuit, and (b) S4T module sub-circuit.

factor of 256 is used to simulate the S4T. Therefore, all the reactive components in the S4T need to be increased by a factor of 256. Selection of reactive components (referred to the HV side) in both HIL simulation and experiment conditions are listed in Table 6.3. The specifications and modeling of sensors in the experiment and QRT HIL are shown in Tables 6.4 and 6.5, respectively.

Table 6.3: Reactive components of the S4T

	Experiment	QRT HIL model
L_m	5 mH	5×256 mH
$L_{leakage}$	5.6 μH	5.6×256 μH
L_r	80 μH	80×256 μH
C_r	6.25 nF	6.25×256 nF
C_f	4.7 μF	4.7×256 μF
XFMR turns ratio	4:1	4:1

6.3.2 Single-module S4T Results

Comparison of HIL simulation and experimental results for a single-module S4T is shown in Figs. 6.8 - 6.10. Fig. 6.8 shows the comparison under steady state. As shown in Fig. 6.8, both-side I_m (blue and red) have similar waveforms and magnitudes. The switching cycle consists of 4 parts: a resonant mode, LV-side charging the transformer, freewheeling period and HV-side discharging the transformer. Therefore, it shows that the state machine operates accurately, the calculation of T_A, T_B, and T_Z are equivalent corresponding to the respective switching frequencies, and the feedback loop performs well to regulate I_m at its reference value. There are some discrepancies in I_m waveforms when the state machine enters the freewheeling mode. This is due to a mismatch in the loop resistances of the freewheeling path on the HV/LV side between the actual power devices in

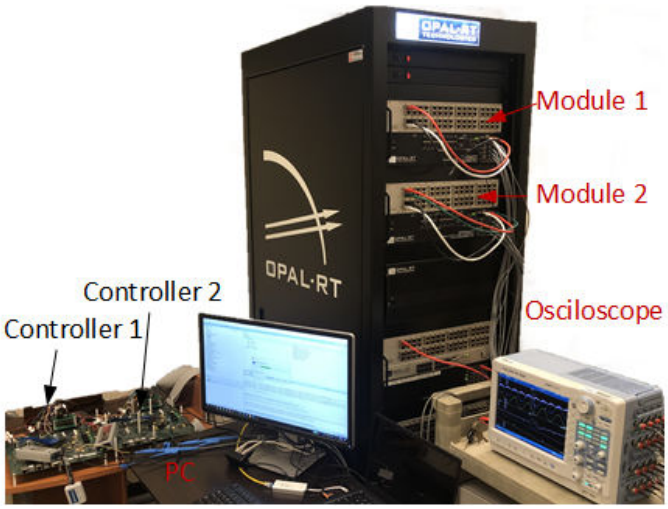
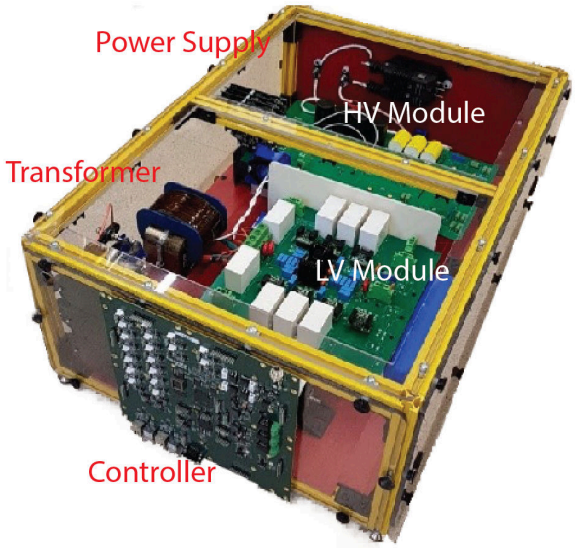


Figure 6.6: Image of implementation of S4T using OPAL RT.



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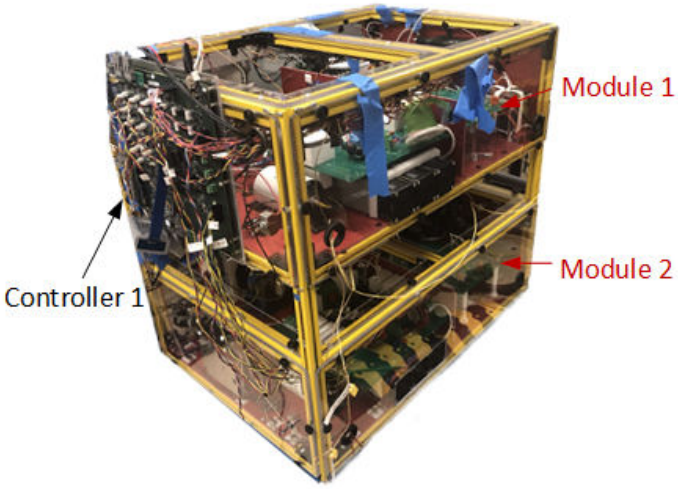


(b)

Figure 6.7: (a) Single-module S4T experimental setup, and (b) two-module M-S4T experimental setup.

the experiment and the device models used in the model. This impacts the current sharing between HV and LV side during freewheeling mode. The operation of the state machine can also be verified from the resonant capacitor voltage (V_{Cr}) (purple in Fig. 6.8(a) and pink in Fig. 6.8(b)). V_{Cr} is varying from high voltage to low voltage, followed by resonance period. From the waveform of V_{Cr}, the controlled dv/dt is achieved and ZVS transition is ensured.

Table 6.4: Sensors of the S4T in Experiment

	Experiment Sensor Gain	Experiment Sensor Bandwidth	Experiment Sensor Delay
HV-side magnetizing current	4.753 / 50	200 kHz	2 μs
LV-side Magnetizing current	4.9 / 200	200 kHz	2 μs
HV-side capacitor voltage	4.375 / 3000	13 kHz	27 μs
HV-side current	4.9025 / 50	100 kHz	2 μs
LV-side current	4.965 / 200	100 kHz	2 μs
LV-side capacitor voltage	5 / 700	500 kHz	2 μs
HV-side capacitor current	4.753 / 50	200 kHz	2 μs

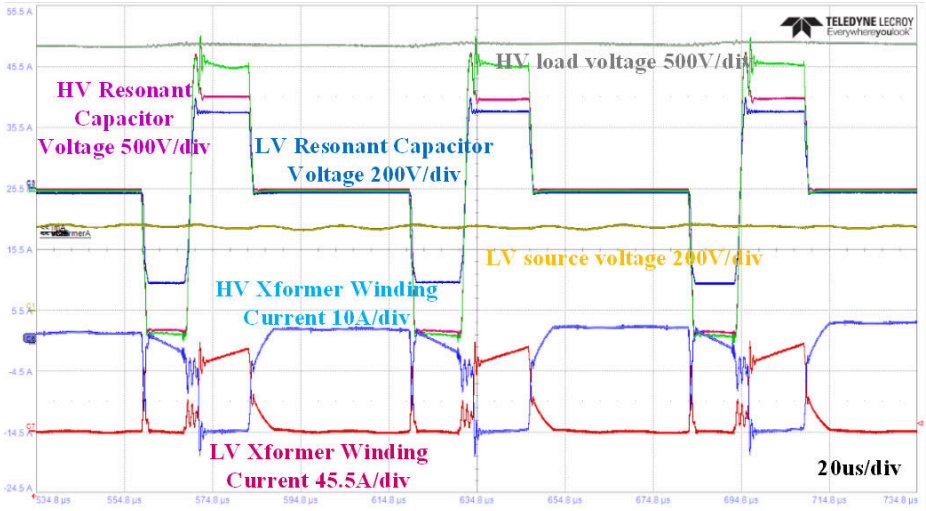
Table 6.5: Sensors of the S4T in QRT HIL model

	QRT HIL Sensor Gain	QRT HIL Sensor Bandwidth	QRT HIL Sensor Delay
HV-side magnetizing current	4.753 / 50	0.78 kHz	512 μs
LV-side Magnetizing current	4.9 / 200	0.78 kHz	512 μs
HV-side capacitor voltage	4.375 / 3000	0.05 kHz	6912 μs
HV-side current	4.9025 / 50	0.39 kHz	512 μs
LV-side current	4.965 / 200	0.39 kHz	512 μs
LV-side capacitor voltage	5 / 700	1.95 kHz	512 μs
HV-side capacitor current	4.753 / 50	0.78 kHz	512 μs

The output and input voltage waveforms are very similar under both conditions, which means all the feedback loops work properly. Fig. 6.10 shows the comparison between the experimental and HIL simulation results when the converter is subjected to a load change. Both results show the decrease in I_m to supply more load current when load increases and recovers to reference value when the load change transient ends. The dynamics of I_m and load current under the load change condition in experimental and HIL-simulated results are closely matched. The time constants of both load currents are equivalent corresponding to the respective switching frequencies. Figs. 6.8 - 6.10 show that the QRT HIL model can represent the real system in terms of simulating the steady-state and transient dynamics.

6.3.3 M-S4T Results

The comparison of HIL simulation and experimental results for a two-module M-S4T is shown in Figs. 6.11 and 6.12. The test condition is at 1.5 kV and 10 kW with 15A mag-



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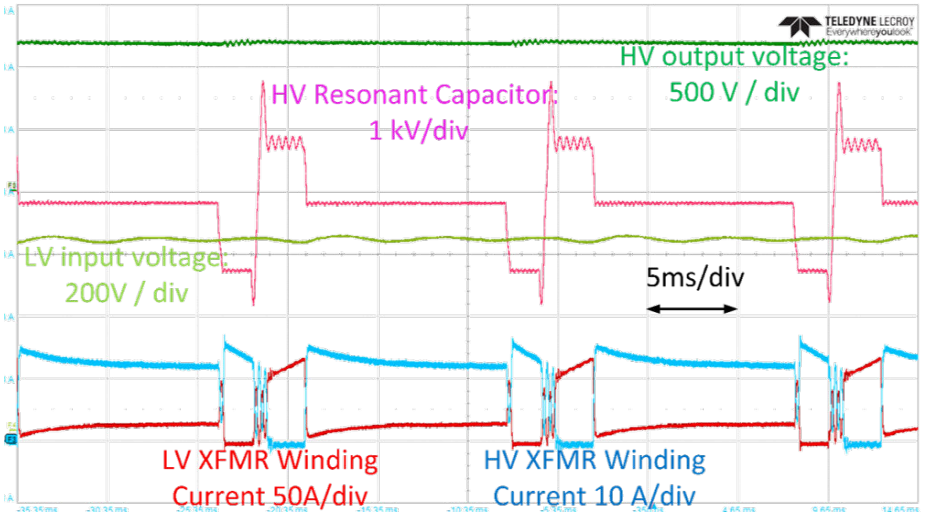
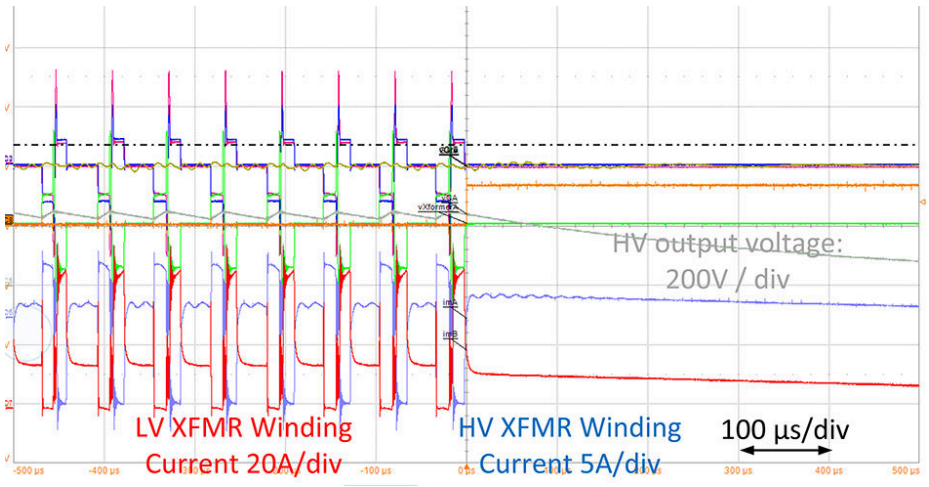


(b)

Figure 6.8: Comparison of converter waveforms in steady state (a) Experiment waveforms and (b) HIL waveforms.

netizing current (referred to HV side). Fig. 6.11 shows the waveforms of a two-module M-S4T under steady state. The LV resonant capacitor voltage, HV resonant capacitor voltage, LV magnetizing current of both modules and HV magnetizing current of both modules are shown in Fig. 6.11. The waveforms of each module are similar to those of single-module operation. Interleaving is achieved for the M-S4T to further reduce the filter size, as shown



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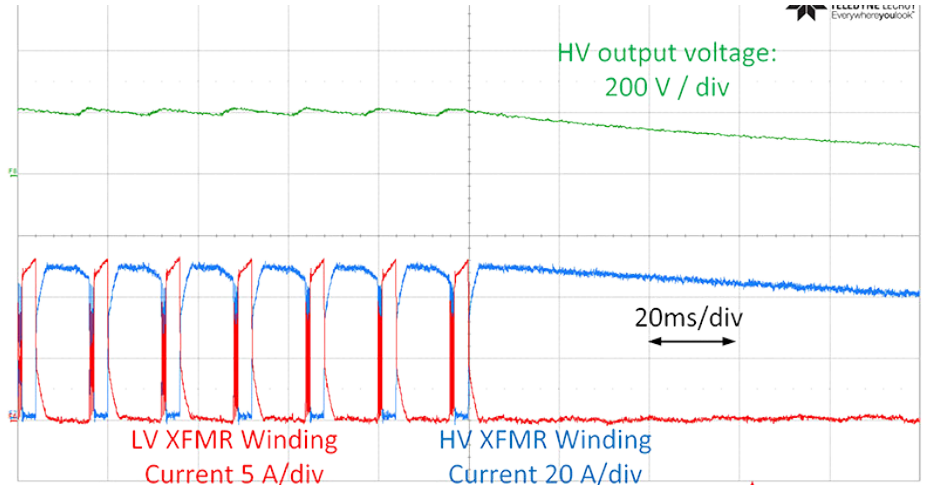
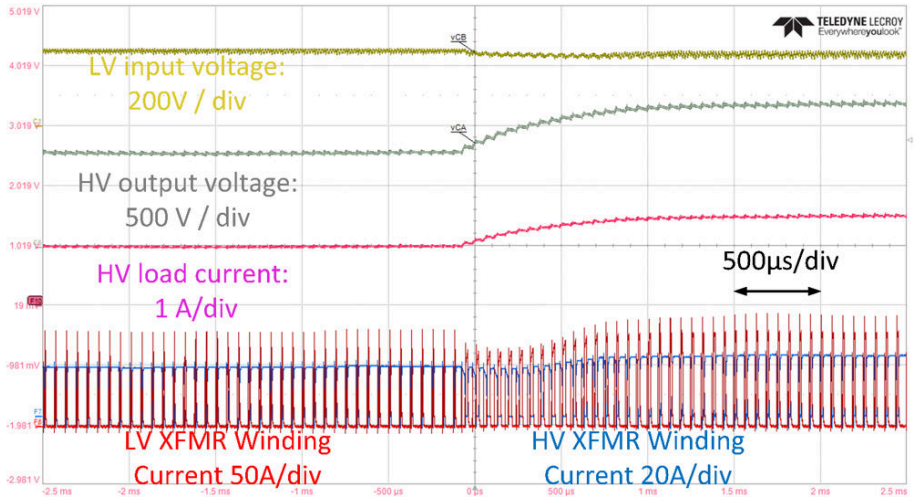


(b)

Figure 6.9: Comparison of load change transient (a) Experiment waveforms and (b) HIL waveforms.

by 180° phase shift between the winding currents and resonant capacitor voltages of both modules. Fig. 6.12 shows the comparison between the experimental and HIL simulation results when the converter is subjected to a load change. As shown in Fig. 6.12, when the load change occurs, the magnetizing currents and HV series-connect side voltages of both



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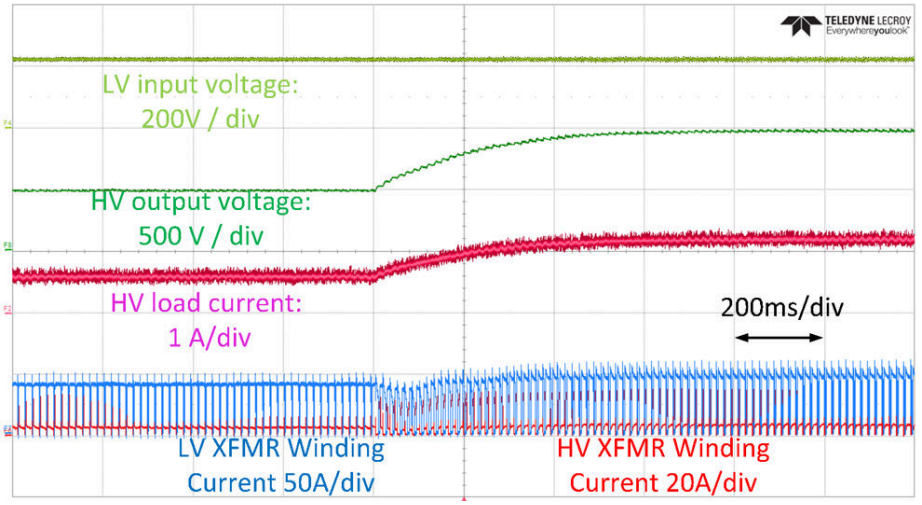
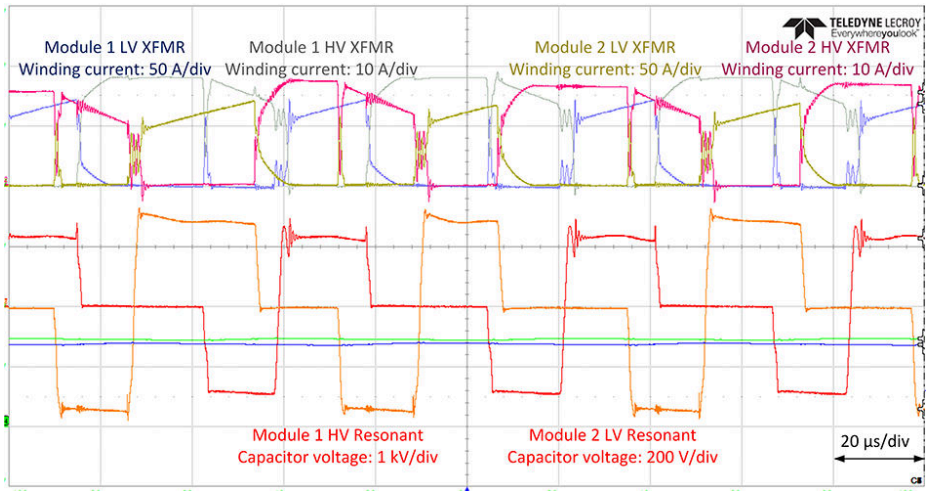


(b)

Figure 6.10: Comparison of load change transient (a) Experiment waveforms and (b) HIL waveforms.

modules are regulated well, which proves the effectiveness of the MPPS when controlling M-S4T.



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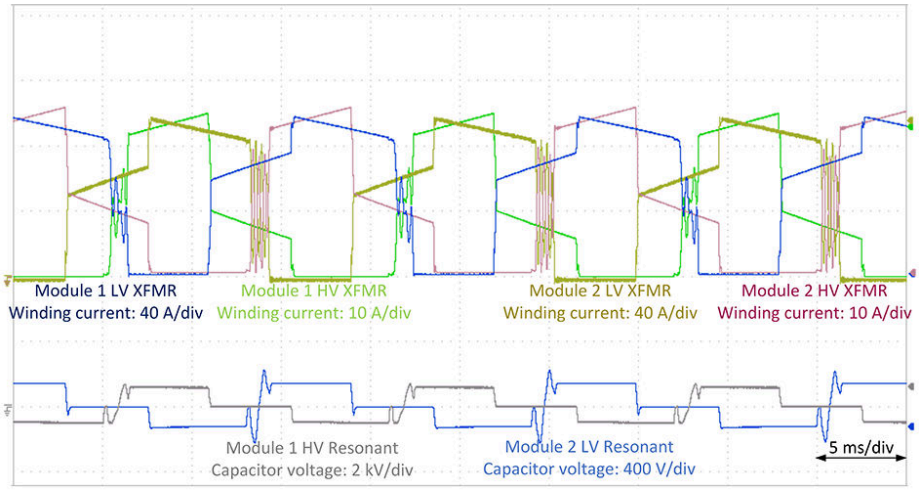
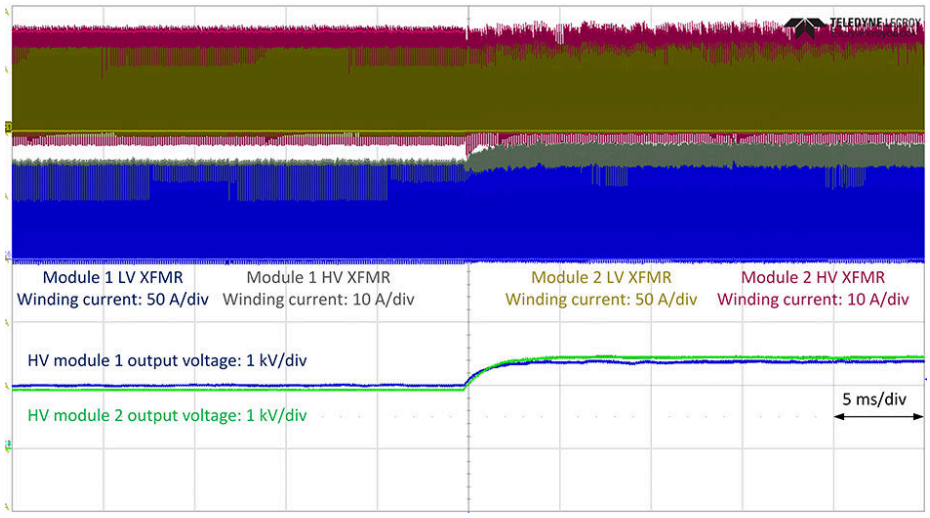


(b)

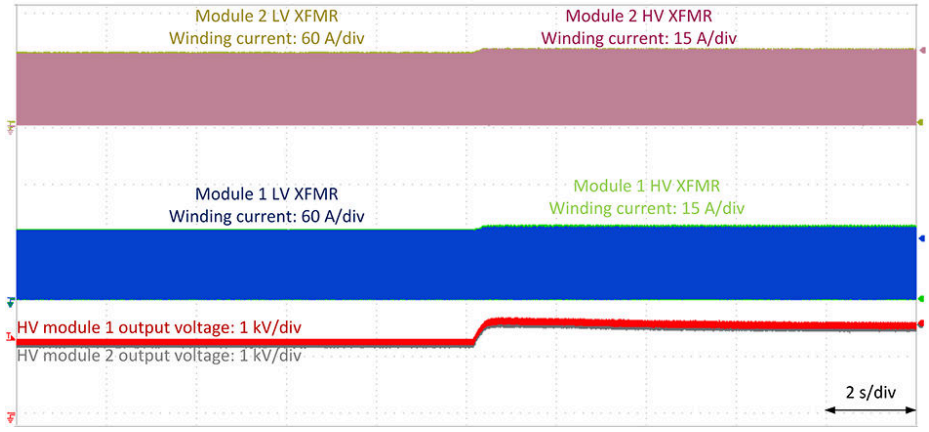
Figure 6.11: Comparison of waveforms of two-module M-S4T in steady state (a) Experiment waveforms and (b) HIL waveforms.

6.3.4 Control Improvement using the HIL Tool

HIL tools not only enable verification of the control algorithm considering non-idealities of the controller but also improve the converter performance. The relative significance of



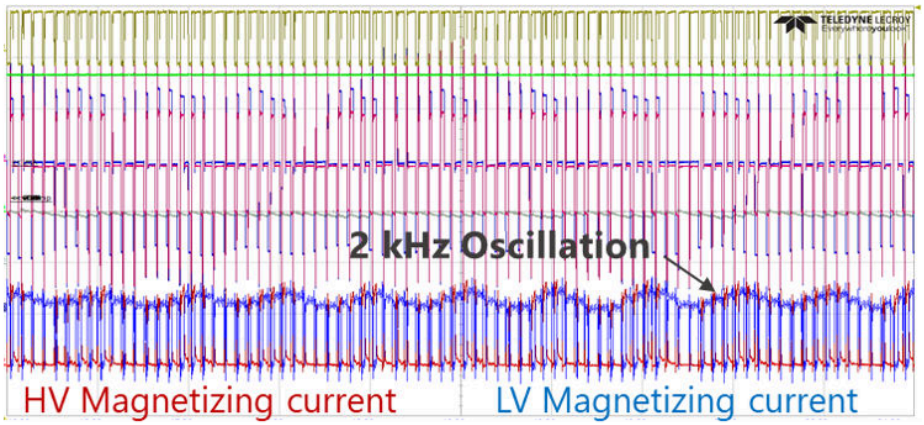
(a)



(b)

Figure 6.12: Comparison of waveforms of two-module M-S4T under load change transient (a) Experiment waveforms and (b) HIL waveforms.

the factors such as sensor and communication delays to the converter performance is understood by using the HIL simulation. This process also helps to design a better set of control parameters for the MPPS. For instance, the delay in the sensor-ADC channel has resulted in an unstable operation due to its interaction with the loop gain, as shown in Fig.6.13.



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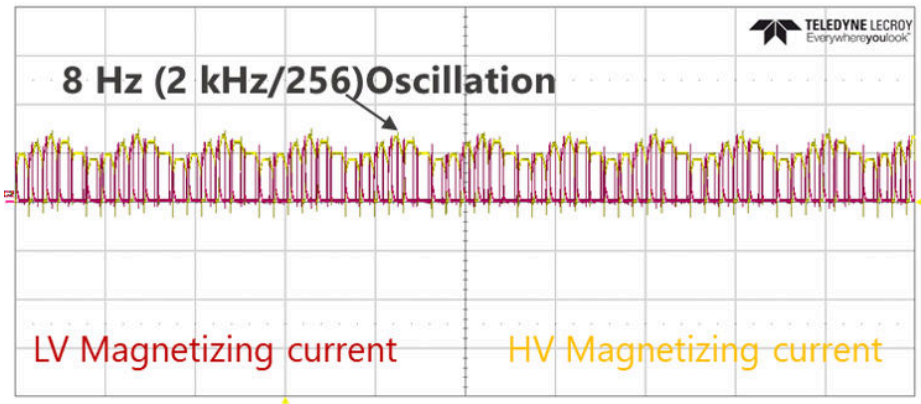


(b)

Figure 6.13: A 2 kHz oscillation on the magnetizing current when the controller is not well-tuned (a) Experiment waveforms and (b) HIL waveforms.

With the help of the HIL simulation, different test conditions can be easily configured, and the cause of the problem can be identified much easier compared to the experimental practice. By understanding the causes of such issues, the performance of the controller can be improved.

6.4 Conclusions

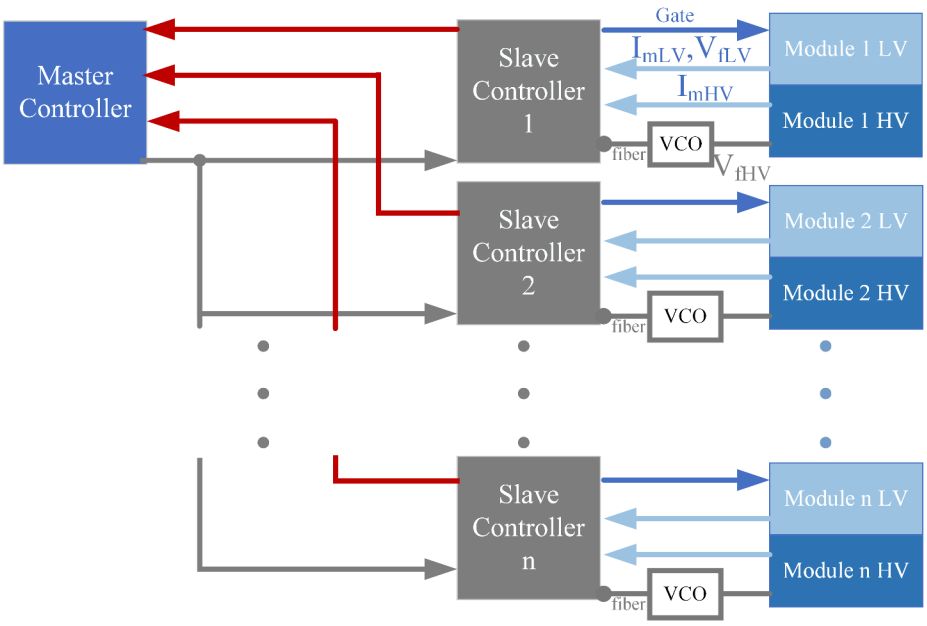
This chapter presents the challenges in (i) modeling of low-inertia converters with resonant operation mode and (ii) implementing of the fast dynamic control using HIL tools. A QRT HIL model is proposed to address the time step limitation when implementing fast dynamic control and solving the low-inertia circuit with resonant operation mode. Non-idealities in the controllers as well as the physical parameters are taken into consideration when simulating with the HIL tools. In addition, a decoupling model is proposed for simulation of modular converters with high device counting. HIL simulation results of an M-S4T under steady-state and transient conditions are compared to the experimental results, showing that the proposed QRT HIL model can simulate the physical converter accurately.

CHAPTER 7
M-S4T CONTROL ARCHITECTURE

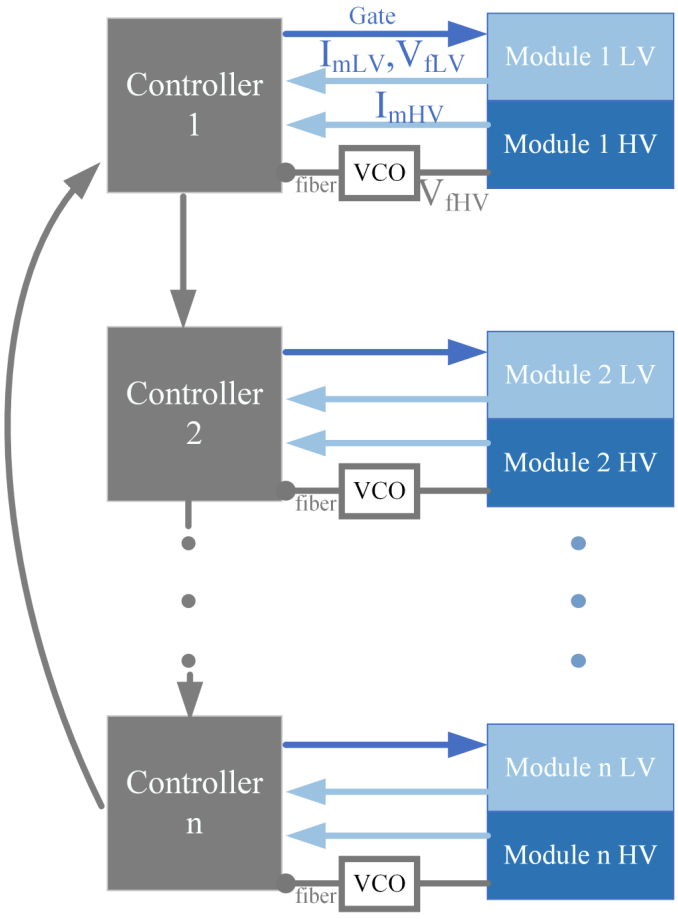
Control architectures based on distributed controllers are favored in control of modular stacked converters because of their scalability, ease of installation and stable structure. However, the existing solutions are only applicable to traditional VSCs with high-inertia components, i.e., larger DC-link capacitance and controlled with slow PI controllers. Therefore, there is no demanding requirement on the communication speed. This chapter presents the challenges in the design of control architecture of low-inertia converters, such as the S4T, particularly using fast-dynamic control. It also proposes a methodology to realize the control architecture for such stacked low-inertia converters. The proposed control architecture is verified on a two-module S4T using HIL simulation in OPAL-RT and in experiments.

7.1 Challenges in S4T Control Architecture

Since the MPPS is a deadbeat-like model predictive-based control method, the sensed/measured and reference values need to be communicated with low latency and refreshed every switching cycle. In addition, the command signals like start-up, shut-down and mode change need fast communication as well to maintain balanced operation between each module. A synchronization signal needs to be communicated to achieve interleaving between different modules. Besides all these signals, a fault (health) signal indicating whether the module is in fault condition or not is required and the fault signal should be set instantaneously once a fault is detected. Depending on the time requirement of all the signals, they can be classified into 2 categories. One set of signals needs to be refreshed at the switching frequency while the other one needs to be refreshed instantaneously. Therefore, at least 2 communication links are needed. Fig. 7.1 shows the topological candidates for each com-



(a)



(b)

Figure 7.1: M-S4T control architecture (a) star topology and (b) ring topology.

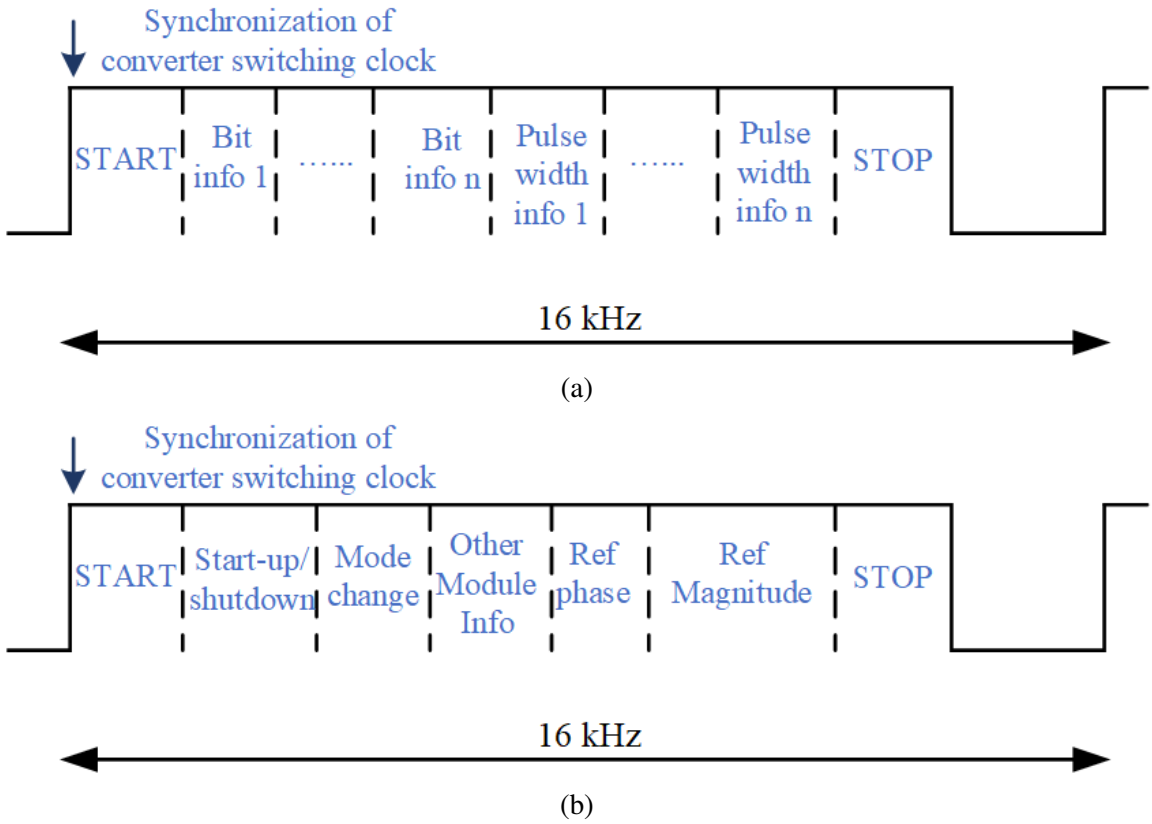
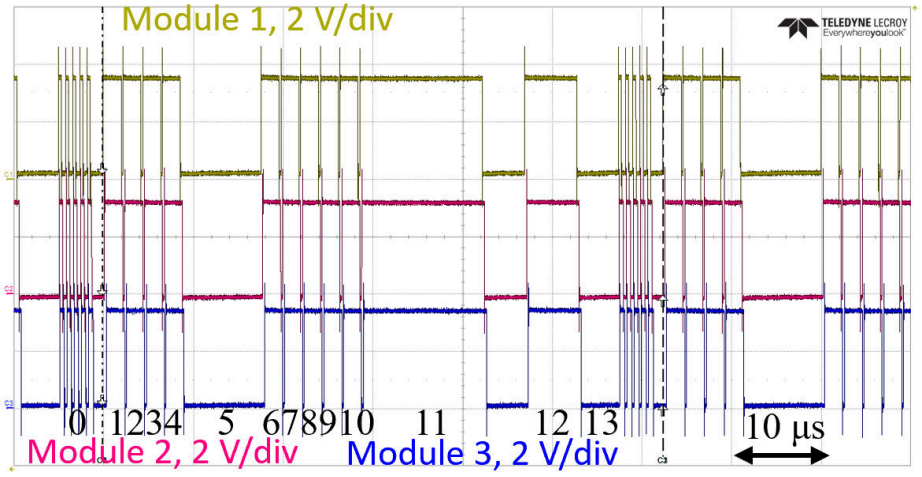
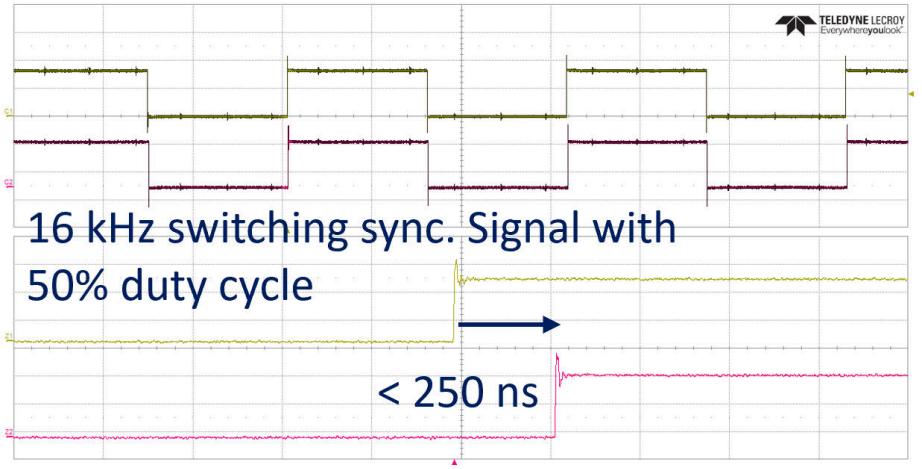


Figure 7.2: (a) General signal package used in the control architecture; (b) a signal package specified for stacked AC application.

munication link. As shown in Fig. 7.1, the star topology (master-slave topology) as well as ring-topology (daisy chain topology) are taken into consideration. Fig. 7.1(a) shows the star topology, in which the hub (master controller) has significantly higher cabling burden compared to other nodes (slave controllers), which makes the implementation complex. Fig. 7.1(b) shows the ring-topology, which features inherent feedback and can be easily configured to check if each controller is acting correctly. In both of the topologies, except the master controller in star topology, all controllers sense control variables and provide gating pulses of its corresponding S4T module. These information are communicated locally within each controller. Although in the ring topology, all the nodes take the risk of breaking the communication chain while only the hub takes the risk in star topology, the inherent feedback can detect any signal breaking and/or shutdown of the converter appropriately. The features including the easy maintenance and scalability of the ring topology



(a)



(b)

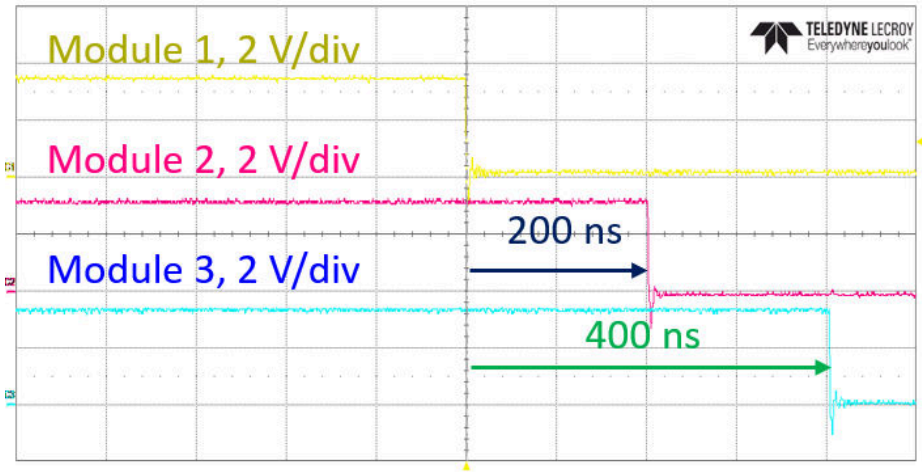
Figure 7.3: Experimental waveform of the (a) signal package for stacked AC application; (b) retrieved switching frequency clock signal; (c) fault signals when a fault occurs.

make it a promising candidate for the control architecture of the S4T.

7.2 Proposed Control Architecture

Based on the discussion in the previous section, a two-link control architecture is proposed. One link is for the information that is refreshed once in each switching cycle while the other one is for the fault (health) signal, which needs to be communicated instantaneously. The function of fault signal is to trigger fault if there is a converter internal fault or loss-of-communication fault. This signal is set to be active-low. However, on the other

link, all the information can be merged and share the same communication link, based on the principle of asynchronous serial communication. Fig. 7.2 shows the conceptual waveform and the information in the asynchronous serial communication link. Generally, as shown in Fig. 7.2(a), the signal package includes start bits, bit information such as start-up/shut-down, mode change, and pulse width modulated signals, which can be used to communicate analog information such as reference voltage magnitude, phase, power reference, etc. The values of these pulse-width signals are proportional to their corresponding pulse widths. For instance, the maximal pulse width of the reference magnitude is 500



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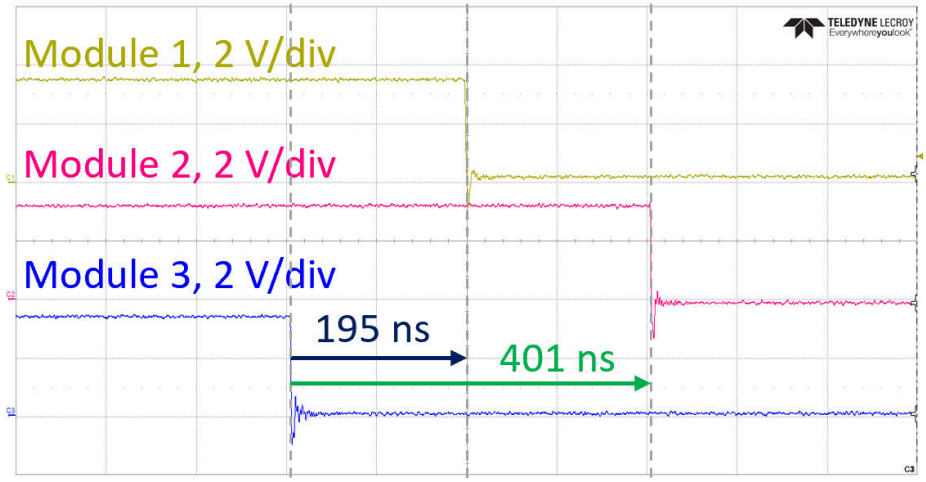


(b)

Figure 7.4: Experimental waveform of fault signal when (a) fault detected by module 1; (b) fault detected by module 3.

Table 7.1: Functionalities of each state in the signal package

	State length	Function	Type
State 0	120 clocks	Start bit	
State 1	120 clocks	Synchronization	
State 2-10	120 clocks each	Command: start up, shutdown	Bit information
State 11	1000 clocks	Reference phase	Pulse width information
State 12	500 clocks	Reference magnitude	Pulse width information
State 13	300 clocks	End bit	

clocks, which corresponds to 3000 V. Then the pulse width is 100 clocks when the reference is 600 V. In Fig. 7.2(b), the signal package for stacked AC application is shown as an example. The signal package is refreshed based on the switching frequency. Fig. 7.3 shows the experimental waveforms of the packaged signal generated by multiple FPGAs, where module 1 is generating the packaged signal while the others receive the signal and propagate the same signal on the communication link. A complete communication signal package consists of state 0 to state 13 as labeled in Fig. 7.3(a) with each communication package getting refreshed at the speed of the switching frequency of the converter. Each switching cycle consists of 3120 FPGA clocks. Table 7.1 summarizes the functionality and state length of each state. Once each module receives the signal, the information in each state is retrieved. Fig. 7.3(b) shows an example of a retrieved 16 kHz switching frequency clock. The latency between the signals is around 200 ns, which is negligible for converter operation. If the number of modules increases and the latency cannot be neglected, a hybrid star-ring topology can be used. Fig. 7.4 shows the fault signals in each module when a fault occurs. The fault types include converter operational fault like over-voltage protection (OVP) and over-current protection (OCP), break of the communication links, failure to start the module, etc. All the modules can set the fault signal to low if a fault is detected. As shown in Figs. 7.4, module 1 and module 3 detect the fault first and set the fault signal to low, respectively. As shown in Figs. 7.4(a), module 2 and module 3 receive the fault signal sequentially. The measured delay of the fault signal is around 200 ns.

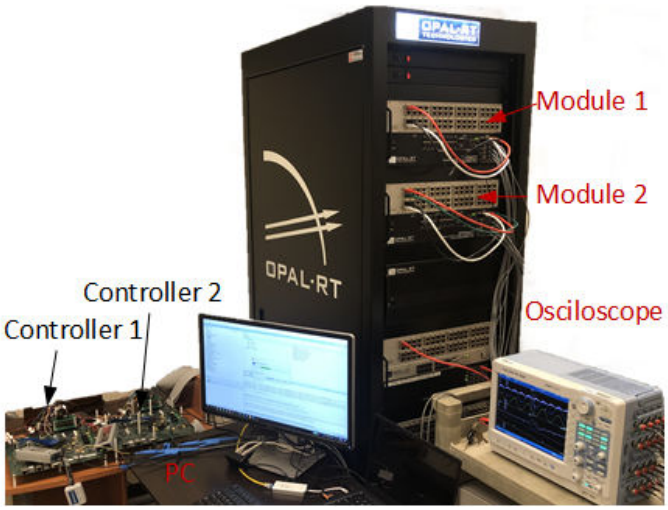
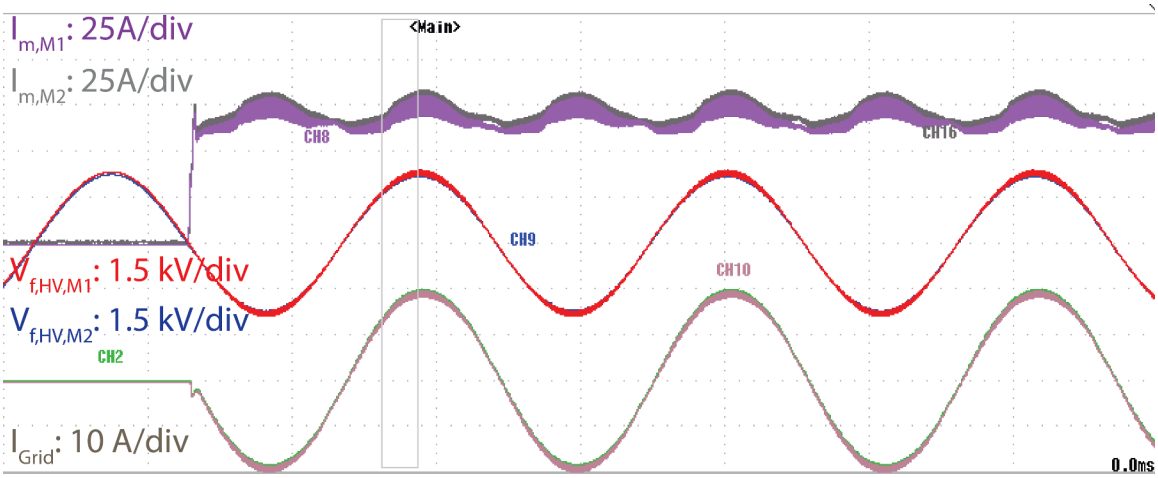


Figure 7.5: Image of implementation of S4T using OPAL RT.

7.3 HIL simulation of M-S4T Control Architecture

Two FPGAs are used to control two S4T modules and linked by the proposed two-wire communication, as shown in Fig. 7.5. The HIL simulation results for a two-module M-S4T using the proposed control architecture are shown in Fig. 7.6. In this simulation, the HV side is interfaced with a single-phase AC grid, which is the same as traction converter. I_m and voltages of HV/LV filter capacitances of both modules are shown in Fig. 7.6. Fig. 7.6(a) shows the waveforms of the M-S4T at start up. I_m in both of the S4T modules are built up simultaneously. In steady state, the waveforms of each modules are similar to those of a single-module operation. Fig. 7.6(b) shows the waveforms when the M-S4T is subjected to a load change. When a load change occurs, I_m and HV series-connect side voltages of both modules are regulated well, thereby verifying the effectiveness of the MPPS and the proposed control architecture. Fig. 7.6(c) shows the zoomed portion of Fig. 7.6(b) subsequent to a load change. Interleaving is achieved for the M-S4T to further reduce the filter size, as shown by 180° phase shift between I_m of both modules.



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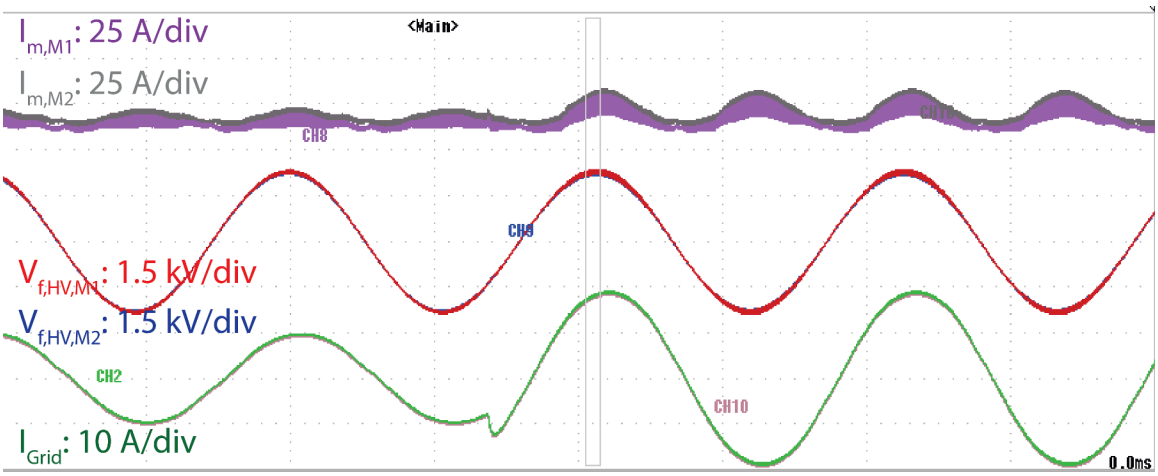

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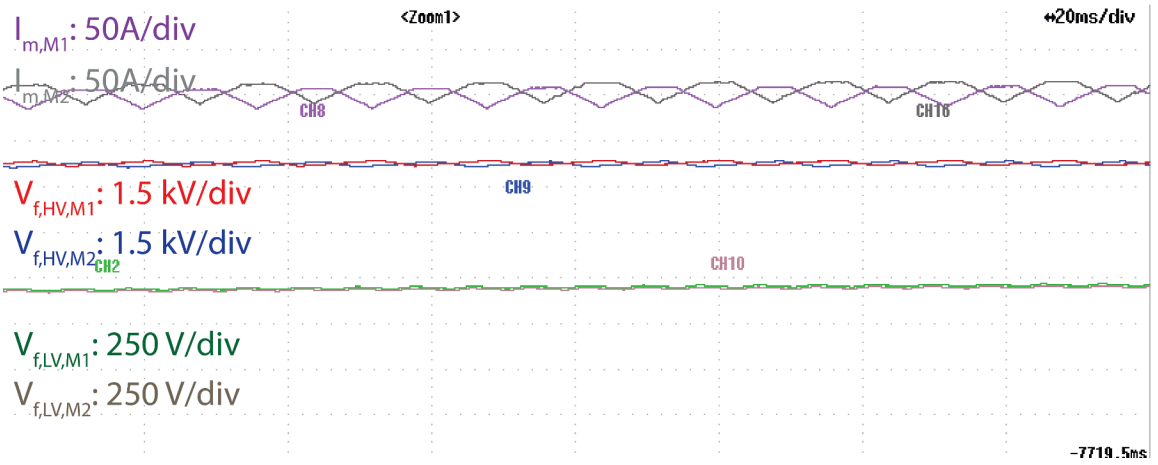


(c)

Figure 7.6: HIL simulation results of a two-module S4T under (a) start-up and (b) step change and (c) zoomed portion of (b).

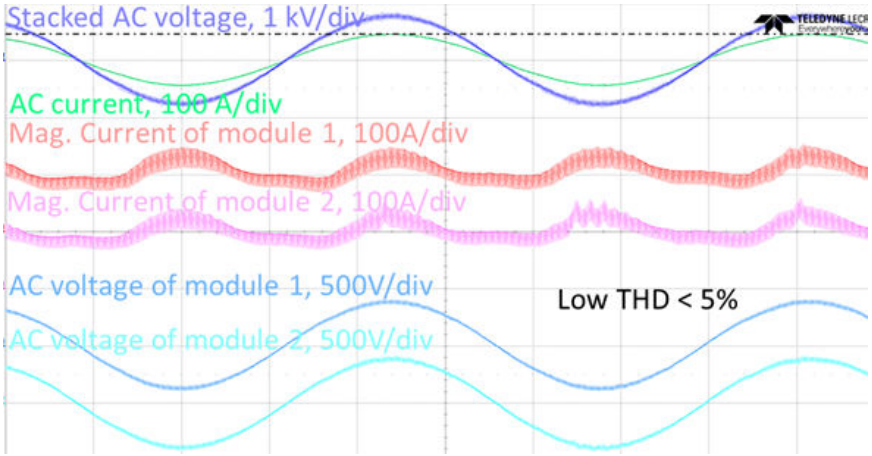
7.4 Experimental Results of M-S4T Control Architecture

Experimental results of a two-module M-S4T using the proposed control architecture is shown in Fig. 7.7(a). The stacked-side RMS voltage is 590 V and the operating power is 20 kW. As shown in Fig. 7.7(a), voltages of both modules are well-balanced and the magnetizing currents of both modules are controlled to track I_m reference. The operating power in each module is also balanced.

Figs. 7.7(b) and (c) show the resonant capacitor voltages of one sub-module. As illustrated in Chapter 3, there are four possible switching sequence in each switching cycle. By selection of the buffer capacitance voltage, the sequence can be simplified. Here only two sequences exist. Fig. 7.7(b) shows the sequence when the buffer port is discharging the magnetizing inductance while Fig. 7.7(c) shows the sequence when the buffer port is charging the magnetizing inductance.

7.5 Conclusions

In this chapter, a new control architecture for low-inertia stacked converters, such as M-S4T is proposed. The proposed control architecture is based on a two-link structure in which one link is to communicate information using serial communication at switching frequency while the other one is for fault information. It is shown that the proposed control architecture can achieve communication latency of 200 ns. The proposed control architecture for the two-module S4T operating at 4 kV, 20 kW is verified using HIL on OPAL-RT platform and also experimentally at 1 kV, 20 kW.



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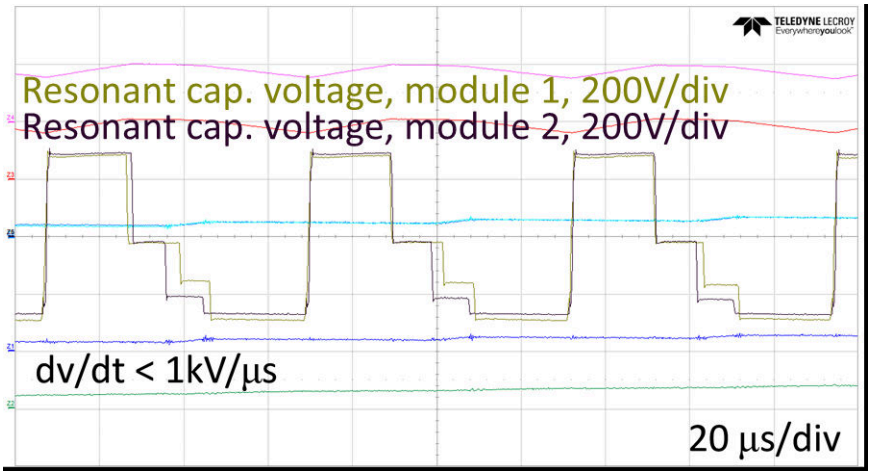

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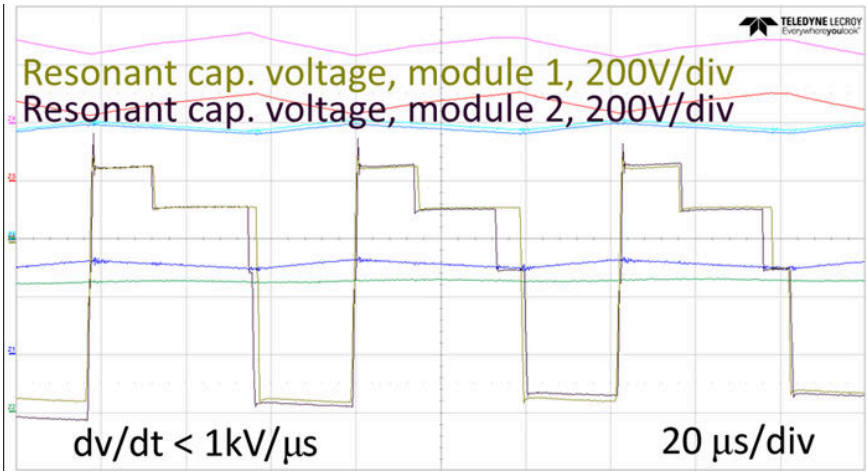


(c)

Figure 7.7: Experimental results of a two-module S4T.(a) steady-state operation (b) resonant capacitance voltage when buffer port charges I_m and (c) resonant capacitance voltage when buffer discharges I_m.

CHAPTER 8
METHODOLOGY FOR DESIGN OF SOFT-SWITCHING SOLID-STATE TRANSFORMER FOR SINGLE-PHASE MVAC-LVAC APPLICATIONS

This chapter investigates the parameter selection of the M-S4T for system-level design. As such, the impacts of parameters such as power level per each module, switching frequency and resonant tank in terms of the efficiency, peak voltage and current stresses as well as the usable portion of the duty cycle or the DC-link utilization are explored. It is shown that the M-S4T design is an intertwined multi-parameter one and for an optimized design, the correlations among the design parameters need to be fully understood. To this end, a detailed loss model of the S4T converter module, especially for the single-phase application, is developed considering the semiconductor devices, the high-frequency transformer as well as the filter components. A generic approach as well as considerations for an optimal selection of design parameters for the M-S4T in the context of a 7.2 kVAC/240 VDC single-phase case used as an example is discussed.

8.1 S4T Design Challenges

The M-S4T design is an intertwined multi-parameter optimization problem. Due to the symmetrical operation of the series-/parallel-connected modules, single module is used in the optimization in this chapter. The correlations among the design parameters including power per module, switching frequency (f_{sw}), resonant capacitance (C_r), and resonant inductance (L_r) need to be fully understood to achieve the optimal design.

In the previous chapters, it has been illustrated that the current in the DC-link magnetizing inductance is proportional to the power transfer capability, i.e., given the input/output voltage level, the higher power per module is processed, the higher the magnetizing current is. The magnetizing current can be optimized for different applications.

8.1.1 Optimal DC-link Current

To maintain a stable operation, a minimum DC-link current level is required. When the operating current level is higher than the minimum current level, free-wheeling state will utilize the remaining duty cycle without energy transfer from the input to the output port during this state. The relationship among the DC-link current level and the input and output current requirements is:

$$I_m = \frac{I_o}{D_o} = \frac{I_{in}}{D_{in}}, \tag{8.1}$$

where I_m is the average value of the magnetizing current, I_{in} and I_o are the input and output currents, respectively. D_{in} and D_o are the input and output duty cycle and satisfy:

$$D_o + D_{in} <= 1, \tag{8.2}$$

AC to DC and DC to DC applications

For DC-DC applications, I_o in (8.1) is a constant value. Therefore, a DC magnetizing current is maintained. The magnetizing current reaches its minimum when the duty cycle of the free-wheeling state is zero.

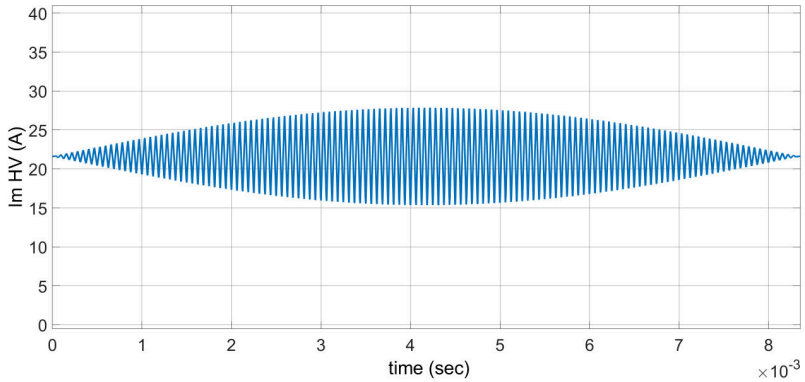
AC to AC applications

In single-phase AC-AC with DC buffer applications, since the instantaneous power transferred with a single-phase AC source varies from zero to 2 p.u., maintaining a maximum DC current to deliver 2 p.u. power is necessary. Although the S4T is able to operate with a constant DC magnetizing current for this application, as shown in Fig. 8.1(a), the efficiency of the converter is compromised. Since I_o in (8.1) varies, I_m can vary corresponding to I_o. This control method, by dynamically varying the I_m level, can effectively reduce the losses in single-phase AC-AC applications. In this method, a varying I_m is applied according to the instantaneous power transferred by the S4T, i.e., the S4T oper-

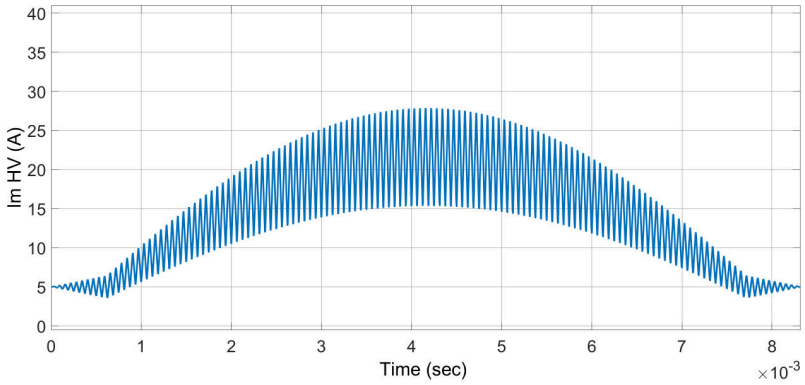
ates with maximum magnetizing current when it delivers 2 p.u. power and operates with minimum magnetizing current when delivering no power, as shown in Fig. 8.1(b).

8.1.2 Optimal Resonant Circuit Design

In the previous chapters, it is shown that soft-switching of the S4T is achieved by ZVS transitions between two active states and free-wheeling state, in which magnetizing current flows through C_r so that the capacitor voltage decreases with a controlled dv/dt. In addition, there is one resonant state in which the resonant capacitor voltage is reset to achieve ZVS for the next switching cycle. In state transition mode, dv/dt is controlled by resonant



(a)



(b)

Figure 8.1: Magnetizing current profile of the S4T for 1-ph AC-AC applications with (a) constant I_m; and (b) varying I_m.

capacitance. In one cycle, the total time used for this mode is:

$$t_{zvs} = \frac{V_{cr(pk+)} - V_{cr(pk-)}}{dv/dt}, \tag{8.3}$$

where $V_{cr(pk+)}$, $V_{cr(pk-)}$ are the positive and negative peaks of the resonant capacitance voltage, respectively. In addition, the resonant state time interval is:

$$t_{res} = \sqrt{L_r C_r}(2\pi - \sin^{-1} \frac{2V_{Cr0} I_m \sqrt{L_r C_r}}{L_r I_m^2 + C_r V_{Cr0}^2}), \tag{8.4}$$

where V_{cr0} is the initial resonant capacitor voltage prior to the resonant mode. t_{zvs} and t_{res} added together contribute to the lost portion of the duty cycle. Intuitively, given the same power level and the same switching frequency, the higher the lost portion of the duty cycle is, the lower the usable duty cycle is. To achieve the same power and charge delivery, the average current in the DC-link magnetizing inductance is increased, by which the component losses and sizing are impacted. Besides, L_r, and C_r in the resonant tank and the leakage inductance of the HF transformer impact the peak device voltage and current stresses, therefore, the overall system design is impacted.

8.1.3 Optimal Switching Frequency

Besides the operating power and resonant tank design, the switching frequency is another key variable in the optimization. Although in the S4T, the switching losses are much reduced compared to the converter that operates under hard-switching condition, the switching losses are still proportional to the switching frequency. In addition, considering the lost portion of the duty cycle due to the ZVS transition and resonant mode is relatively fixed, a higher switching frequency will result in less usable duty cycle per switching cycle.

To optimally design the S4T converter for a given application, the interactions of the factors including dv/dt, usable portion of the duty cycle, the voltage and current stresses, and the losses need to be analyzed based on the control and operation. A higher switching

frequency helps in size and weight reduction of the converter, but the usable portion of the duty cycle decreases since t_{zvs} and t_{res} is fixed by the selection of resonant tank. Therefore, higher I_m is required to deliver the same power, which results in the increased losses. Increasing C_r results in reduced stresses and dv/dt, but the usable portion of the duty cycle decreases because t_{zvs} and t_{res} increase. This can be compensated by either increasing I_m or decreasing f_{sw} to deliver the same amount of power. However, the losses of the converter and the peak current stress will be increased as a consequence. The interactions like these need to be understood and a methodology is needed to optimally design the S4T converter.

8.2 Power Loss Modeling

As discussed in the previous section, power losses play a key role in understanding the interactions between different design parameters. To calculate the power losses in the S4T, a comprehensive loss model comprising of: i) semiconductor device model; ii) transformer model; and iii) filter model is presented.

8.2.1 Semiconductor Device Model

Semiconductor device losses contribute to a major part of the total converter losses. Although the power losses of a switching device are comprised of conduction and switching losses, in the S4T, due to its current source nature and negligible switching losses, conduction losses contribute to the major part of the total losses. Considering all the power devices used in the S4T including the main switching devices, auxiliary resonant devices, the leakage management devices on both HV and LV sides, the conduction losses can be calculated by:

$$P_{cond} = V_f \times I_d, \tag{8.5a}$$

$$V_f = V_{f0} + R_{d0} \times I_d. \tag{8.5b}$$

where I_d is the instantaneous current in the device, V_f is the forward voltage drop of the reverse-blocking (RB) device, V_{f0} and R_{d0} are the RB-device forward characteristics acquired from device datasheet including both active device (IGBT or MOSFET) and diode considering temperature impact. The switching losses of the S4T are negligible but not exactly zero. The characterization of RB devices is discussed in detail in Chapter 4. The turn-off loss is proportional to the controlled dv/dt, which is related to the selected resonant capacitance.

8.2.2 HF Transformer Model

The design of HF transformer for the S4T is application dependent and the methodology is discussed in [96]. For the use of the S4T in MV applications with specific basic insulation requirements, coaxial winding consisting of an inner Litz wire for HV side and an outer tinned-copper braid for LV side is considered to meet the desired insulation level with minimal leakage inductance. The loss in the HF transformer depends on the magnetizing current waveform and the switching frequency. Nano-crystalline is selected as the core material for which, the core loss per unit volume is calculated using:

$$\frac{W}{m^3} = 7180 \times 1.09 \times (f_{sw})^{1.62} \times (\Delta_B)^{1.98}\,, \tag{8.6a}$$

$$\Delta B = B_{\max} \times \frac{0.5 \times I_{pp}}{I_{M_{avg}} + 0.5 I_{pp}} \tag{8.6b}$$

$$I_{pp} = \frac{V_{in\_pk} * K_d}{L_M \times 2 \times F_s} \tag{8.6c}$$

The AC resistance factors to calculate the copper loss in the Litz winding for HV side and copper braid for LV side are calculated using the following equations:

$$AC_{loss} = (\frac{I_{pp}}{2} \times 0.577)^2 \times F_R \times R_{DC} \times D \tag{8.7}$$

where F_R and D represent the AC resistance factor and active energy transfer time, respectively.

8.2.3 Filter Model

To meet the grid requirements on harmonics, each module requires a filter capacitance. The LC filter is found suitable for most of the application of the S4T. The filter inductance may vary depending on the application and user requirements. Therefore, only the power loss in the filter capacitance is considered. The equivalent-series-resistance (ESR) of the filter capacitance extracted from the datasheet is used to calculate the corresponding loss.

8.3 Optimal Selection of Design Parameters

This section presents the interaction and correlation of different design parameters and a method to optimally select the required parameters based on the application. A 50 kVA 7.2 kV/240 V single-phase solid-state transformer is taken as an example. This section assumes a linearized and simplified approach in calculating the voltage and current stresses, which suffices to optimally select the design parameters.

8.3.1 Selection of Rated Power per Module

The first goal is to optimize the operating power per each module and to come up with the total number of required modules, considering the overall efficiency (η), usable portion of the duty cycle (D_{eff}) as well as stresses (V_{pk}, I_{pk}). The S4T features a controlled dv/dt, and the upper limit of dv/dt is set as 2.5 kV/μs in this example to utilize the advantages of S4T in terms of EMI reduction. The upper limit of the voltage peak is set as 500 V when using 650 V devices on the LV side and the upper limit of the current stress is set as three times the rated current of the device since the peak current occurs only for several μs within one switching cycle.

The flowchart of this optimization procedure is shown in Fig. 8.2. The maximum

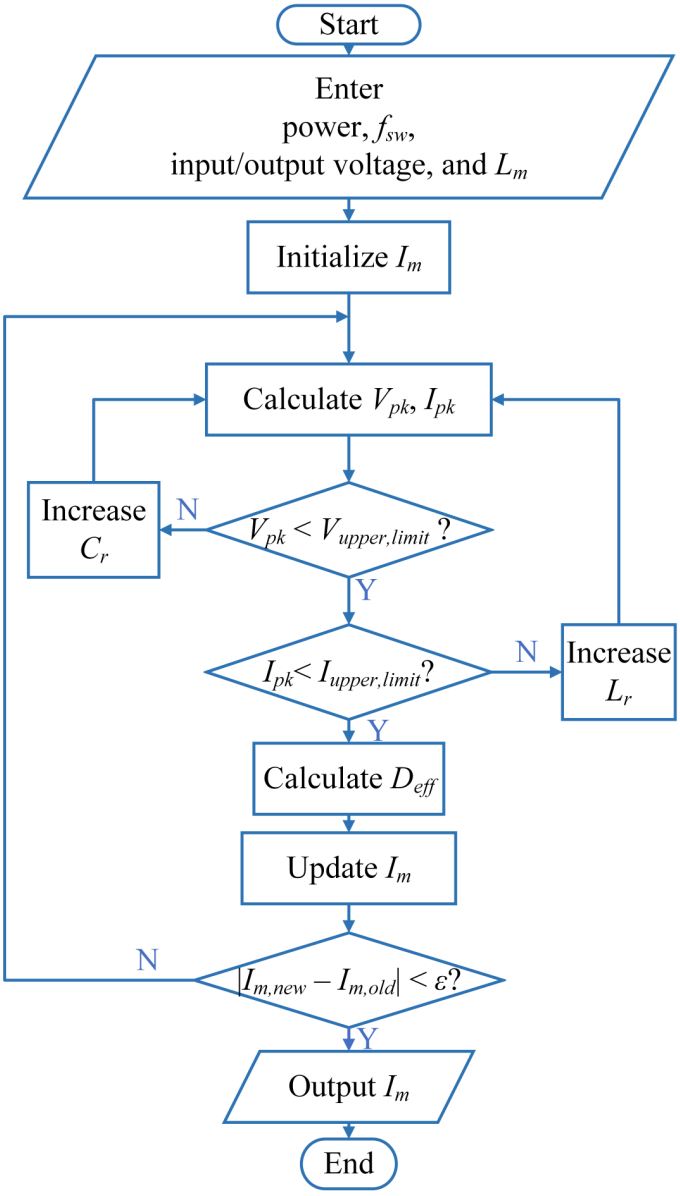
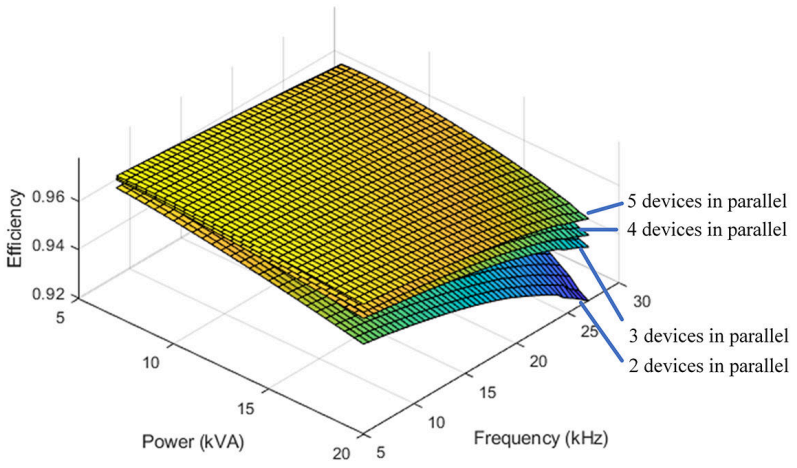
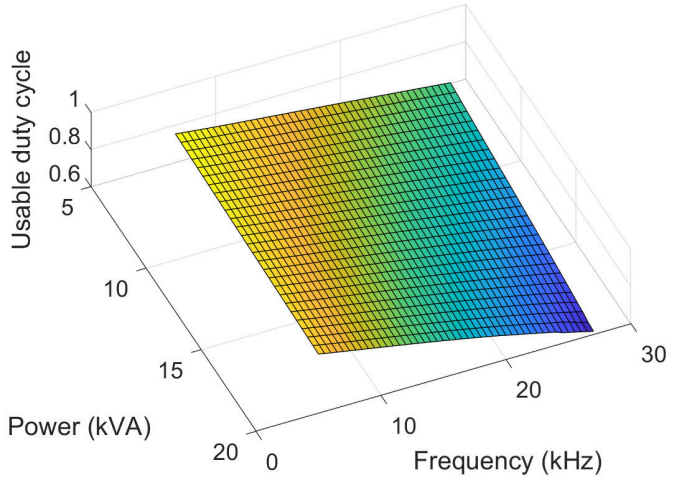


Figure 8.2: The flowchart used to select I_m and C_r.

average magnetizing current and the resonant capacitance are calculated iteratively, and the lost portion of the duty cycle is calculated correspondingly. The relationships/couplings among η , D_{eff}, V_{pk}, I_{pk}, power/module, and f_{sw} are shown in Figs. 8.3 and 8.4. As shown in Fig. 8.3(a), while delivering higher power, more devices should be used in parallel to meet the device thermal requirements, otherwise, efficiency decreases dramatically when power increases. As shown in Figs. 8.3(a) and (b), when f_{sw} increases, the usable portion



(a)



(b)

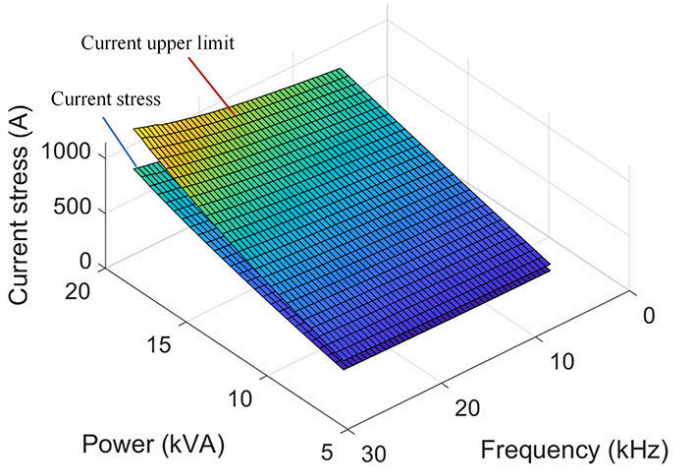
Figure 8.3: Relationship among power/module, f_{sw} and (a) η and (b) D_{eff}.

of the duty cycle decreases, which results in a higher magnetizing current required for the same power level. Therefore, it is highly inefficient to design with high power/module and operate with high f_{sw}. As shown in Fig. 8.4(a), the peak current is below the upper limit throughout the power or frequency sweeps. However, as shown in Fig. 8.4(b), to maintain the voltage stress below its upper limit, the power/module needs to be reduced. The design choices are such that (i) the switching frequency is between 10 kHz to 22 kHz, (ii) maximum power/module is realized with a fewer number of devices used, (iii) a higher portion of the duty cycle is used, and (iv) the efficiency is at least 96.5%. Therefore, 10 kW

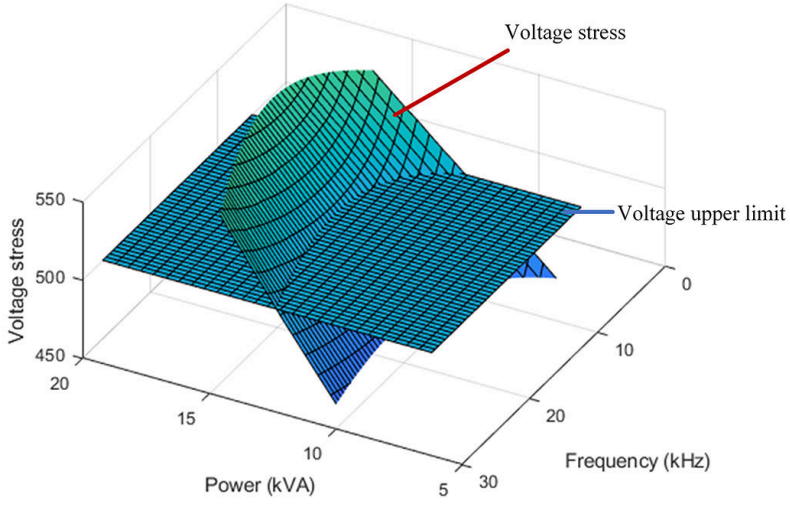
power/module is considered the optimal choice for this application.

8.3.2 Selection of the Switching Frequency and the Resonant Capacitance

With 10 kW/module selected and the switching frequency in the range of 10 kHz to 22 kHz, Fig. 8.5 presents the correlations among f_{sw} as well as the corresponding resonant capacitance with the power losses, dv/dt, D_{eff}, V_{pk}, and I_{pk}. As shown in Figs. 8.5(b) and 8.6(b), at least a 0.22 μF C_r is required on the LV side to meet the required dv/dt and safe operation in terms of voltage stress while the impact of f_{sw} is minor. The peak current

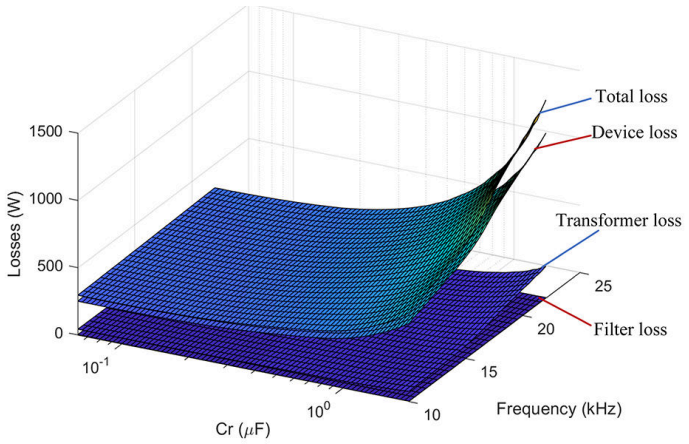


(a)

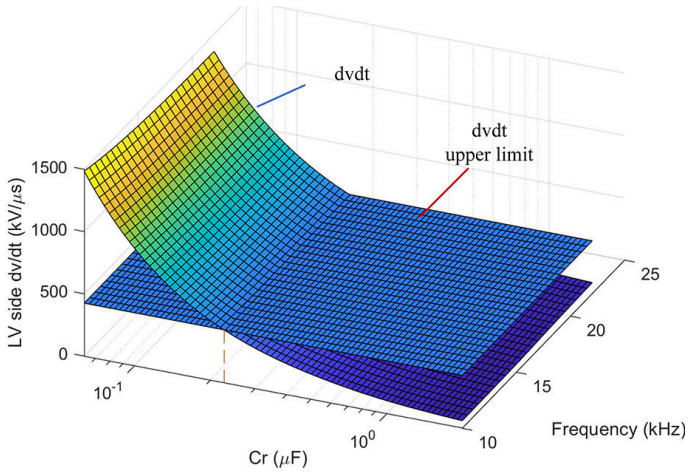


(b)

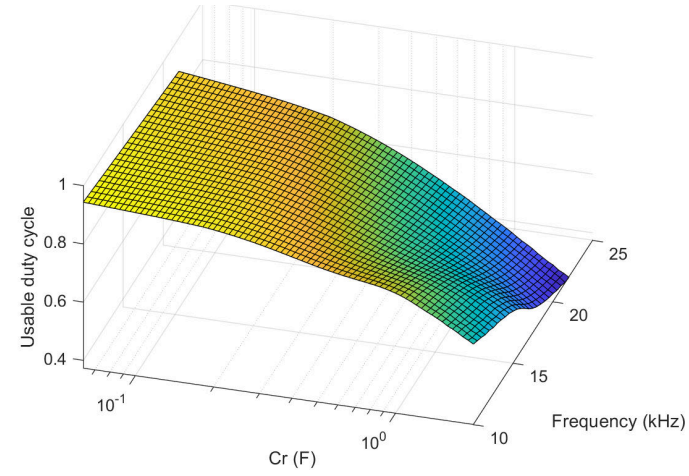
Figure 8.4: Relationship among power/module, f_{sw} and (a) I_{pk} and (b)V_{pk}.



(a)

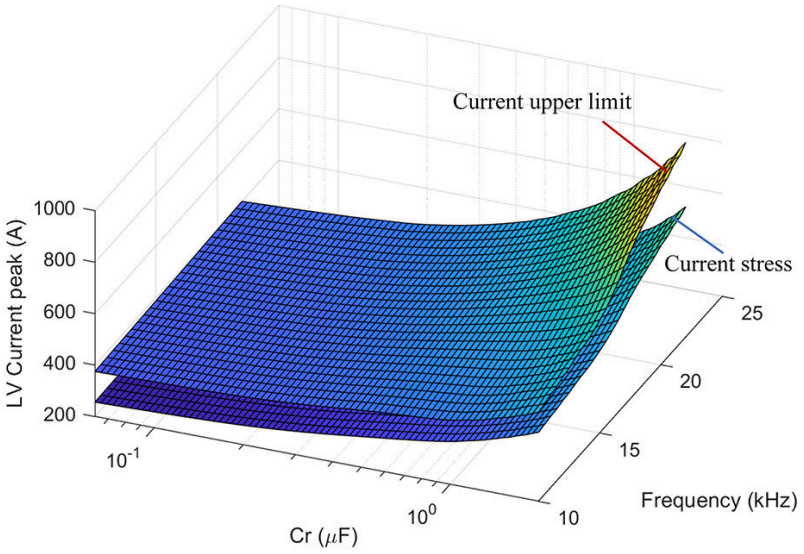


(b)

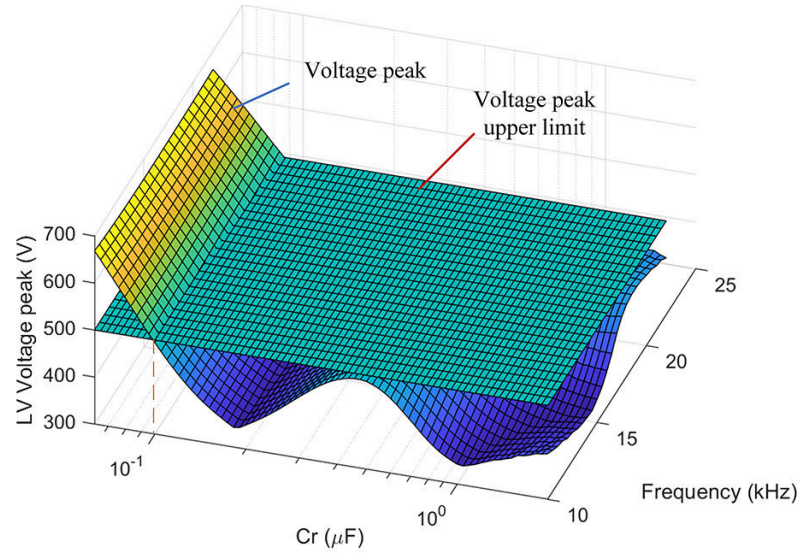


(c)

Figure 8.5: Relationships among C_r, f_{sw} and (a) power losses, (b)dv/dt and (c) D_{eff}.



(a)



(b)

Figure 8.6: Relationships among C_r, f_{sw} and (a) I_{pk} and (b)V_{pk}.

is always below the upper limit. A switching frequency of 16 kHz is considered optimal for this application and the selected power level with the objective of lower power losses, higher usable portion of duty cycle while all the parameters are within the constraints. Fig. 8.7 shows the relationship between the efficiency and load level when the S4T delivers power to the grid, using the selected values of C_r = 0.23 μF. For this case, the efficiency of the S4T at full-load and 40$\%$ load is 96.5$\%$ and 91.6$\%$, respectively.

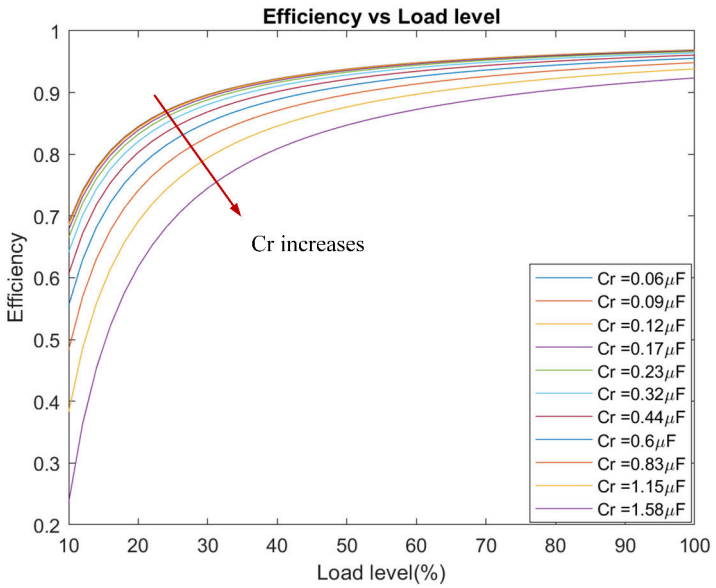


Figure 8.7: Relationship among C_r, η and load level.

8.4 Conclusions

This chapter presents a comprehensive loss model of the S4T considering device losses, transformer losses and filter losses. The chapter investigates the impact and correlation of power level per each module, switching frequency and resonant capacitor selection on the system efficiency, voltage and current stresses as well as the usable portion of duty cycle. An optimal selection of design parameters is proposed based on the considerations and trade-offs of the aforementioned parameters.

CHAPTER 9

SCALING TO FULL-SCALE TRACTION CONVERTERS

In Chapter 3, an M-S4T with DC buffer capacitor configuration is proposed for the next-generation traction converter, as shown in Fig. 9.1. From Chapter 4 to 8, multiple key aspects of the M-S4T are investigated and discussed. Although the power and voltage level used in the proposed research are lower compared to the full-scale traction converters for locomotives and high speed trains, all the methodologies used in the proposed research and the corresponding conclusions are applicable to the full-scale traction converters.

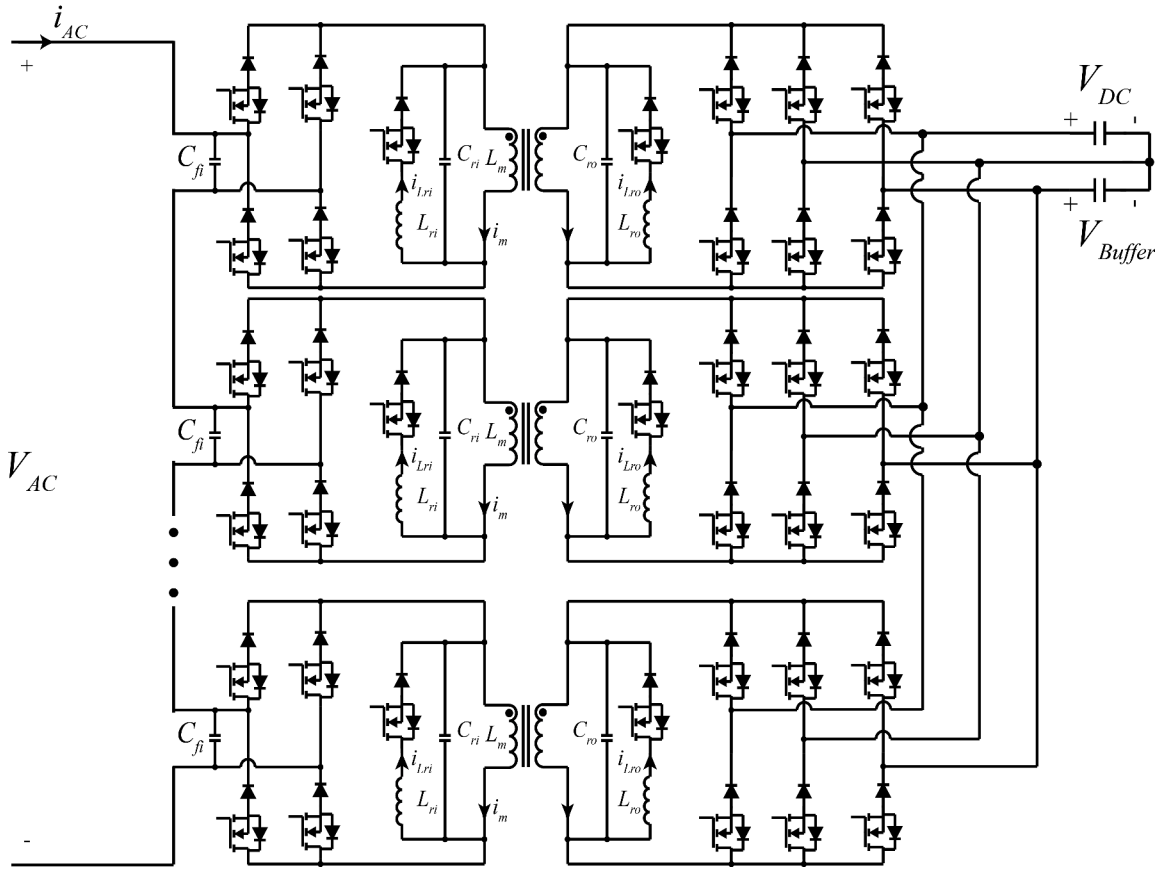


Figure 9.1: Circuit diagram of the AC-DC configuration of the M-S4T with DC buffer capacitor.

9.1 Characterization of the RB SiC devices

In the proposed traction converter as shown in Fig. 9.1, all of the devices used in the converter are RB devices. Although a specific RB SiC device is characterized in Chapter 4, the loss mechanism is the same when higher power RB SiC devices are used. Based on the conclusions from Chapter 4, when an RB device is used in a ZVS-CSC, the voltage sharing phenomenon occurs, which results in additional switching losses. In addition, soft-switching technique helps to reduce the majority of switching losses and control the dv/dt.

9.2 Practical Concerns of using RB Devices in S4T

The proposed gating strategy of the S4T in Chapter 5 is independent from the power and voltage levels, as shown in Fig. 9.2. The same gating strategy can be directly applied to a full-scale traction converter to eliminate additional voltage stresses on the devices and ensure ZVS for all the devices.

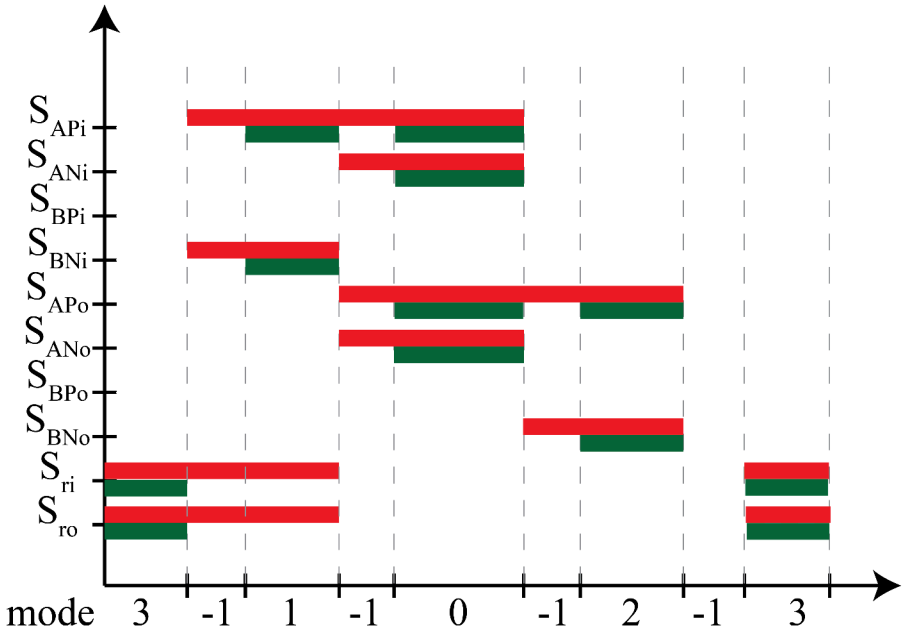


Figure 9.2: The proposed switching sequence of the S4T for general cases.

9.3 Real-Time Modeling of the M-S4T

As shown in Fig. 9.3, the power and voltage level does not play a role in the proposed decoupled QRT HIL model in Chapter 6. By using the decoupled model, eighteen S4T modules can be simulated on the existing OPAL-RT platform.

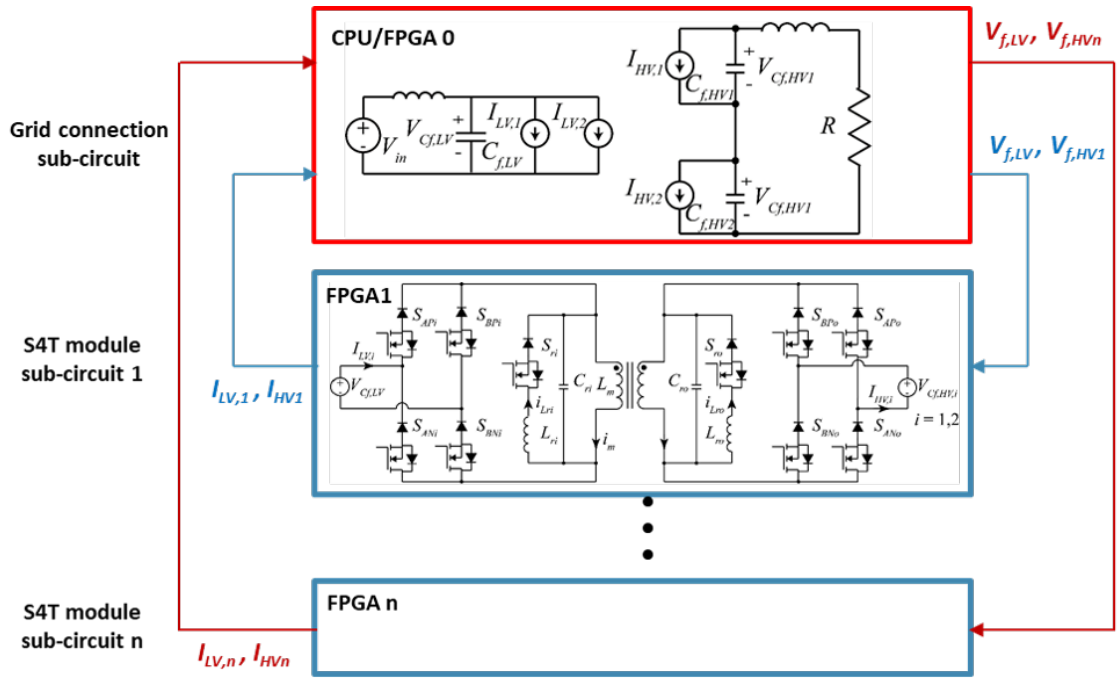


Figure 9.3: Decoupled M-S4T circuit for HIL simulation.

9.4 M-S4T Control Architecture

The proposed control architecture is demonstrated on three controllers and the latency between the adjacent controllers is verified to be less than 250 ns. In a full-scale nine-module stacked M-S4T, the communication latency between the first and the last S4T modules is less than 2 μs, which is acceptable to the M-S4T control.

9.5 Methodology for Design of the S4T

The design process shown in Fig. 9.4 is applicable to an S4T module with any power and voltage levels. Using this methodology, the optimal power per module, f_{sw} and reso-

nant tank design can be selected.

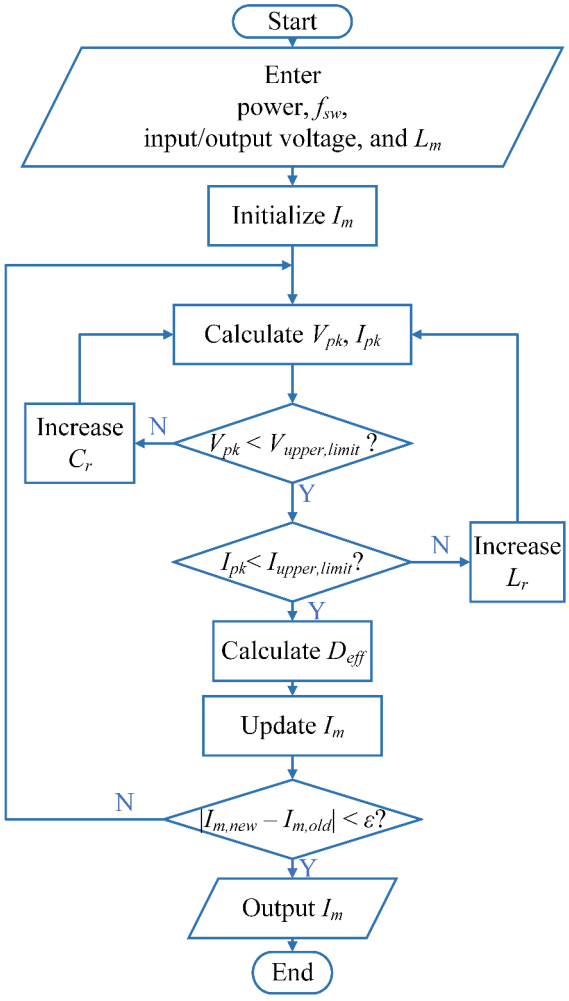


Figure 9.4: The flowchart used to select I_m and C_r.

9.6 Summary

In this chapter, it is shown that the proposed methodologies and conclusions can be applied to a full-scale traction converter although the power and voltage level used in the proposed research are lower compared to the full-scale traction converters.

CHAPTER 10
CONCLUSIONS, CONTRIBUTIONS AND FUTURE WORK

10.1 Conclusions

This dissertation presents deep investigation of the M-S4T for traction applications including practical concerns of power devices, verification of control, design of control architecture as well as optimization of the converter.

Chapter 3 presents all of the configuration options of the M-S4T for traction applications. It is shown that the single-phase AC to DC configuration with a DC buffer capacitor is more flexible with less control complexity compared to the other configurations.

Chapter 4 presents the detailed test results and model extraction for 3.3 kV 45 A SiC module with five RB devices in the package. A novel test-bed was designed and built for this characterization and model extraction of RB modules under both hard-switching and ZVS conditions. The testing helps to generate parasitic and loss models for the RB devices, showing that switching losses are reduced by as much 96%, while dv/dt is reduced from 30 kV/μs to $<$ 1 kV/μs. The testing also helps to identify the unexpected dynamic voltage sharing issues between the series diode and MOSFET. It was shown that this voltage sharing issue within an RB module (between the switch and the diode) results in a marginally higher switching losses.

In Chapter 5, it was shown that the same phenomenon of dynamic voltage sharing, when extended to two RB modules (one upper RB module and one lower RB module) in the S4T, causes additional voltage stress (up to 1.5 pu) across each RB module. Modified switching schemes to limit this voltage stress when the RB modules are used in such converters are presented and verified through an S4T prototype rated at 1.5 kV, 10 kVA. In addition, a proper switching scheme for resonant switches are also discussed to reduce the voltage

stresses.

Chapter 6 presents the challenges in modeling of low-inertia converter with resonant operation mode and implementing of the fast dynamic control using HIL tools. A QRT HIL model is proposed to address the time-step limitation when implementing fast dynamic control and solving the low-inertia circuit with resonant operation mode. Non-idealities in the controllers as well as the physical parameters are taken into consideration when simulating with the HIL tools. In addition, a decoupling model is proposed for simulation of modular converters with high device counting. HIL simulation results of an M-S4T under steady-state and transient conditions are compared to the experimental results, showing that the proposed QRT HIL model can simulate the physical converter accurately.

In Chapter 7, a new control architecture for low-inertia stacked converters, such as M-S4T is proposed. The proposed control architecture is based on a two-link structure in which one link is to communicate information using serial communication at switching frequency while the other one is for fault information. It is shown that the proposed control architecture can achieve communication latency of 200 ns. The proposed control architecture for the two-module S4T operating at 4 kV, 20 kW is verified using HIL on OPAL-RT platform and also experimentally at 1 kV, 20 kW.

Chapter 8 presents a comprehensive power loss model of the S4T considering device, transformer and filter losses. The chapter investigates the impact and correlation of power level per each module, switching frequency and resonant capacitor selection on the system efficiency, voltage and current stresses as well as the usable portion of duty cycle. An optimal selection of design parameters is proposed based on the considerations and trade-offs of the aforementioned parameters.

Chapter 9 presents the application of the proposed methodologies and conclusions to a full-scale traction converter although the power and voltage level used in the proposed research are lower compared to the full-scale traction converters.

10.2 Contributions

The following tasks have been completed:

- Characterization of the RB devices used in the M-S4T using a novel DPT under both hard-switching and soft-switching conditions;
- Comparison of the switching losses under both hard-switching and soft-switching conditions and identification of loss mechanisms during switching transients;
- Investigation of a proper gating scheme for all RB devices in the M-S4T to reduce the switching losses and EMI;
- QRT HIL modeling of the M-S4T for verification of fast dynamic control algorithms of low-inertia converters and accelerated simulation;
- Modeling of large-scale S4T for HIL simulation using decoupled circuit model;
- Design and verification of the control architecture and communication used to control the M-S4T using the proposed QRT HIL model on OPAL-RT platform;
- Development of the comprehensive S4T loss model;
- Optimization of the system level parameters including power per module, switching frequency, etc.

10.3 Future Work

There are several research directions that could be further explored based on the results presented in this work:

- Investigation of the behavior of the M-S4T under typical conditions and faults on the system such as voltage sags, arcing, faults as well as converter module failure;

- Investigation of the systematic protection of the M-S4T in terms of hardware-based protection scheme including the converter-level protection and gate driver-level protection as well as software-based protection scheme;

- Incorporating the cost of components in the optimization process. The cost of components could impact the overall design and their selection.

- Investigation of control and design of the single phase S4T with smallest buffer capacitance, i.e., an AC capacitance.

- Investigation of control and design of the single phase S4T with direct driving capability, i.e., 3 phase AC output.

Appendices

PUBLICATION LIST

Journal paper

[1] X. Han, L. Zheng, R. P. Kandula, K. Kandasamy, D. Divan and M. Saeedifard, "Characterization of 3.3 kV Reverse-Blocking SiC Modules for Use in Current-Source Zero-Voltage-Switching Converters," *IEEE Transactions on Power Electronics*.

Conference papers

[2] X. Han, R. P. Kandula, K. Kandasamy, D. Divan and M. Saeedifard, "Soft-Switching Characterization of 3.3 kV Reverse-blocking SiC Devices," in *IEEE 6th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, 2018, pp. 185–191.

[3] X. Han, L. Zheng, R. P. Kandula, K. Kandasamy, M. Saeedifard and D. Divan, "Real-Time Modeling and HIL Simulation of Stacked Low-Inertia Converters with Soft-Switching and Fast Dynamic Control,"in *Proc. IEEE Energy Convers. Congr. Expo.*, 2019.

[4] X. Han, L. Zheng, Z. An, R. P. Kandula, M. Saeedifard, and D. Divan, "Design of Control Architecture for Stacked Low-Inertia Converters with Fast Dynamic Control," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2020.

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